FPGA-BASED HARDWARE REALIZATION FOR 4G MIMO WIRELESS SYSTEMS

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Key words: MIMO; Alamouti; FPGA; testbed

Abstract: Emerging multiple-input multiple-output (MIMO) systems are called to play a key role in fourth generation (4G) wireless systems in order to achieve higher data rate and advanced spectral efficiency. Even with extensive research on the design of transmission and reception algorithms, little is known about the complexity of hardware implementation. The MIMO encoder design and implementation is straight forward, however, the decoder implementation is little more complex as it requires resource utilization. This paper presents an efficient hardware realization of MIMO systems that utilizes the resources of the device by adopting the technique of parallelism. The hardware is designed and implemented on a Xilinx Virtex™-4 XC4VLX60 Field Programmable Gate Arrays (FPGA) device. In this paper, a comprehensive explanation of the complete design process is provided, including an illustration of the tools used in its development. The results are obtained for 2×2 MIMO system for coding and decoding at the transmitter and the receiver. The system is developed based on modular design which simplifies system design, eases hardware update and facilitates testing the various modules in an independent manner.

Izvedba 4G MIMO brezžičnega sistema na osnovi FPGA vezij

Kjučne besede: MIMO, Alamouti, FPGA, testiranje

Izvleček: Več-vhodni in **več-**izhodni (MIMO) sistemi bodo igrali pomembno vlogo v 4. generaciji (4G)brezžičnih sistemov za prenos podatkov z visoko hitrostjo. Čeprav se že izvajajo obsežne raziskave na področju načrtovanja oddajnih in sprejemnih algoritmov, se le malo ve o kompleksnosti izvedbe strojne opreme. Zasnova in izvedba MIMO kodirnika je enostavna, a je implementacija dekodirnika bolj zapletena. V članku je predstavljena učinkovita izvedba strojne opreme MIMO sistema z vzopredenjem virov naprave. Strojna oprema je zasnovana in izvedena na Xilinx Virtex™-4 XC4VLX60 FPGA vezju. Prav tako je v članku predstavljen proces načrtovanja vezja z ilustracijo pripomočkov, ki so bili uporabljeni pri razvoju. V prispevku so prikazani rezultati za 2x2 MIMO sistem za kodiranje in dekodiranje na oddajni in sprejemni strani. Sistem je zasnovan na osnovi modularnega načrtovanja, ki poenostavi načrtovanje celega sistema, olajša posodobitev strojne opreme in olajša testiranje posameznih modulov.

1. Introduction

The use of multiple antennas, usually referred as multiple-input multiple-output (MIMO) systems, has gained overwhelming interest during the last decade—both in academia and industry. MIMO systems have evolved rapidly as a generic technology that promises to be a strong contender for 4G wireless systems to accomplish multiplexing gain, diversity gain, or antenna gain, thus enhancing the bit rate, the error performance, or the signal-to-noise-plus-interference ratio of wireless systems, respectively without increasing total transmission power or bandwidth /1, 2/. Recent progress in MIMO standardization and prototyping has forced manufacturers worldwide to pay more attention to implementation aspects. Theoretical performance analysis and simulations of a system confirm predictions under idealistic conditions, but to validate the performance in a practical environment, a testbed is essential as many imperfections of the real world are neglected in simulations /3/. Testbeds have traditionally been implemented on general-purpose and sequential Digital Signal Processors (DSP) or on Application Specific Integrated Circuits (ASIC). Enhanced algorithms, which are generally highly parallelizable, and higher data transmission rates can burden DSP beyond its capacity for real-time processing /4/. Although ASIC is fast and power-efficient, its implemented designs are inflexible /5/ and productions are time-consuming and extremely expensive. To overcome the drawbacks of DSP and ASIC, one hardware platform that has become very popular for design, prototyping and validation of such digital signal processing algorithms is Field Programmable Gate Arrays (FPGA). Unlike ASIC, FPGA is reconfigurable, that is, their internal structure is only partially fixed at fabrication, leaving the wiring of the internal logic to the application designer for the intended task. FPGA allows control over parallelism in resource utilization and also the measurement of resource utilization and power consumption.

The design and implementation of MIMO testbeds have become more and more attractive to researchers as has been observed in the past few years /3, 6, 7, 8/. Rao et al. put forward a classification scheme for different types of testbeds /9/. The simplest approach they recognized is targeted towards burst mode transmissions, and offline signal processing. This design minimizes the cost; however it severely limits the scenarios in which the testbed can be used, because the signal processing is not done in real-time. Real-time FPGA design and implementation of MIMO testbed has received a significant attention in recent years. Different practical implementation aspects of real-time MIMO testbed are presented in /10/ and /11/. A real-time MIMO processing platform is developed by Dowle et al. which can be used to investigate different space-time algorithms /4/. The hardware implementation of a low complexity decision feedback equalization detection method for MIMO systems is described by Yu et al. /12/. In /13/ an FPGA based hardware module is designed for MIMO decoding that is embedded in a prototype of a 4G mobile receiver. These systems are designed based on sequential processing and hence resource is not properly utilized. The main scope of this paper is to present the design and implementation of an FPGA based 2×2 MIMO testbed that not only provides a faster and real-time solution but also the hardware is similar to the final deployment environment. The rest of the paper is organized as follows; Section 2 introduces the 2×2 MIMO system model. This is followed by a hardware design description of the MIMO testbed in Section 3. Section 4 discusses hardware implementation of the testbed. Finally the paper is concluded in Section 5.

2. MIMO System Model

The goal of a good wireless communication system is to provide a reliable link between the transmitter and the receiver. Since a wireless link is affected by multipath fading, scattering and shadowing /15/, a severely attenuated and distorted transmitted signal may arrive at a receiver. Recent research on wireless systems shows that MIMO is effective to reduce the fading effect in the wireless channel by providing diversity /16/ and this improves BER performance in receiver.

Alamouti /17/ presented a remarkable spatial and time diversity scheme for MIMO transmission that improves quality of the received signal by using simple processing scheme at the transmitter and linear decoding at the receiver. In a classical one-transmitter system, symbols S_0, S_1, S_2 ... are transmitted at symbol periods *t*, *t+T*, *t+2T*, ... respectively. In a two transmitter Alamouti scheme, however, the symbols S_0 and S_1 are transmitted simultaneously from two transmit antennas Tx_1 and Tx_2 respectively, at symbol period *t*. At the next symbol period *t+T*, Tx_1 transmits symbol $-S^*_1$ and Tx_2 transmits symbol S^*_0, where * represents the complex conjugate. Table 1 presents an example of encoding and transmission sequence for four symbols and two transmit antenna scheme.

Table 1. Data transmission format of Alamouti scheme

	Time Intervals			
	t	$t+T$	$t+2T$	$t+3T$
Tx_1	s_0	$-s_1^*$	s_2	$-s_3^*$
Tx_2	s_1	s_0^*	s_3	s_2^*

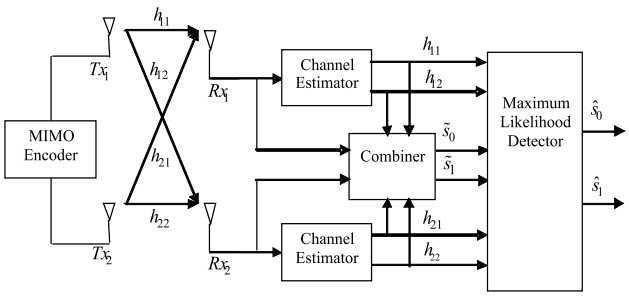

Fig. 1: Block diagram of MIMO system

The channels between the transmit and receive antennas are h_{11}, h_{12}, h_{21} and h_{22} respectively as mentioned in Fig. 1. A low complexity channel estimator can be used to successfully approximate the channel at the receiver, as described in /14/. The received signal can be expressed as

$$\mathbf{R=HS+W} \quad (2)$$

Where H is the channel response matrix and W is additive white Gaussian noise (AWGN). The received signals at time *t* are

$$\text{at receive antenna one: } r_1 = h_{11}s_0 + h_{21}s_1 + w_1 \quad (3)$$

$$\text{at receive antenna two: } r_3 = h_{12}s_0 + h_{22}s_1 + w_3 \quad (4)$$

The signals received at time *t+T* are

$$\text{at receive antenna one: } r_2 = -h_{11}s_1^* + h_{21}s_0^* + w_2 \quad (5)$$

$$\text{at receive antenna two: } r_4 = -h_{12}s_1^* + h_{22}s_0^* + w_4 \quad (6)$$

w_1, w_2, w_3, and w_4, are complex Gaussian random variables representing noise and interference. Alamouti states that the transmitted symbols S_0 and S_1 can be estimated in a maximum likelihood fashion by first combining the received signals according to the following equations

$$\tilde{s}_0 = h_{11}^* r_1 + h_{21} r_2^* + h_{12}^* r_3 + h_{22} r_4^* \quad (7)$$

$$\tilde{s}_1 = h_{21}^* r_1 - h_{11} r_2^* + h_{22}^* r_3 - h_{12} r_4^* \quad (8)$$

and then using a standard maximum likelihood detector to attempt to recover S_0 and S_1 from $\tilde{s}_0$ and $\tilde{s}_1$.

3. Design of a MIMO System

This section illustrates the hardware design of a 2 x 2 MIMO system. The hardware is designed in modular fashion in order to simplify system design. The main emphasis is led on the ability to extend the hardware in an easy way if the

system requires hardware updates. The MIMO system can be broadly divided into two parts: the transmitter and the receiver.

3.1. MIMO Transmitter

Alamouti scheme for two transmit antennas is used in this system design which outputs two streams of symbols and the outputs are fed to identical transmit chains. The transmit module of the design consists of four small sub-modules: MIMO encoder, selection block, in-phase and quadrature (*I-Q*) modulator and a numerically controlled oscillator.

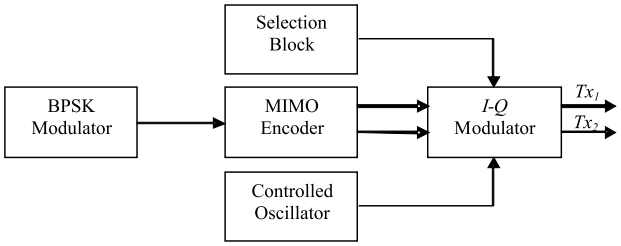

Fig. 2: Transmitter design of a MIMO system

Fig. 2 shows the system architecture to implement a real-time, continuously operating two transmit antenna Alamouti scheme. The BPSK modulated symbols are encoded into space-time code in MIMO encoder. The output of the encoding process is two streams of modulated symbols. Each stream is fed to identical transmit chain each driving a separate antenna. A selection block is used to indicate the symbol period. Depending on the symbol period, symbols are selected from the encoder. Carrier signals are generated by numerically controlled oscillator which comprises a look-up table and a counter. The *I-Q* carriers are generated which are multiplied with encoded symbols to perform *I-Q* modulation. Adding together the *I* and *Q* components, the corresponding symbols are generated and they are then transmitted through transmit antennas.

3.2. MIMO Receiver

Hardware design and implementation of the MIMO receiver is based on equations (7) and (8). However the complex values and their operations of the equations cannot be simply implemented using hardware description language (HDL). Hence the complex values are expanded to real and imaginary parts to simplify implementation. The resulting expressions are shown in equations (9) to (12).

$$\begin{aligned} s0re = {} & \mathrm{Re}(h_{11})\times \mathrm{Re}(r_1) + \mathrm{Im}(h_{11})\times \mathrm{Im}(r_1) + \\ & + \mathrm{Re}(h_{12})\times \mathrm{Re}(r_2) + \mathrm{Im}(h_{12})\times \mathrm{Im}(r_2) + \\ & + \mathrm{Re}(h_{21})\times \mathrm{Re}(r_3) + \mathrm{Im}(h_{21})\times \mathrm{Im}(r_3) + \\ & + \mathrm{Re}(h_{22})\times \mathrm{Re}(r_4) + \mathrm{Im}(h_{22})\times \mathrm{Im}(r_4) \end{aligned} \quad (9)$$

$$\begin{aligned} s0im = {} & \mathrm{Re}(h_{11})\times \mathrm{Im}(r_1) - \mathrm{Im}(h_{11})\times \mathrm{Re}(r_1) - \\ & - \mathrm{Re}(h_{12})\times \mathrm{Im}(r_2) + \mathrm{Im}(h_{12})\times \mathrm{Re}(r_2) + \\ & + \mathrm{Re}(h_{21})\times \mathrm{Im}(r_3) - \mathrm{Im}(h_{21})\times \mathrm{Re}(r_3) - \\ & - \mathrm{Re}(h_{22})\times \mathrm{Im}(r_4) + \mathrm{Im}(h_{22})\times \mathrm{Re}(r_4) \end{aligned} \quad (10)$$

$$\begin{aligned} s1re = {} & \mathrm{Re}(h_{12})\times \mathrm{Re}(r_1) + \mathrm{Im}(h_{12})\times \mathrm{Im}(r_1) - \\ & - \mathrm{Re}(h_{11})\times \mathrm{Re}(r_2) - \mathrm{Im}(h_{11})\times \mathrm{Im}(r_2) + \\ & + \mathrm{Re}(h_{22})\times \mathrm{Re}(r_3) + \mathrm{Im}(h_{22})\times \mathrm{Im}(r_3) - \\ & - \mathrm{Re}(h_{21})\times \mathrm{Re}(r_4) - \mathrm{Im}(h_{21})\times \mathrm{Im}(r_4) \end{aligned} \quad (11)$$

$$\begin{aligned} s1im = {} & \mathrm{Re}(h_{12})\times \mathrm{Im}(r_1) - \mathrm{Im}(h_{12})\times \mathrm{Re}(r_1) + \\ & + \mathrm{Re}(h_{11})\times \mathrm{Im}(r_2) - \mathrm{Im}(h_{11})\times \mathrm{Re}(r_2) + \\ & + \mathrm{Re}(h_{22})\times \mathrm{Im}(r_3) - \mathrm{Im}(h_{22})\times \mathrm{Re}(r_3) + \\ & + \mathrm{Re}(h_{21})\times \mathrm{Im}(r_4) - \mathrm{Im}(h_{21})\times \mathrm{Re}(r_4) \end{aligned} \quad (12)$$

If these equations are directly converted into HDL and synthesized, they use up most of the resources available on the FPGA of the testbed. In order to overcome the problem a new design is considered as shown in Fig. 3. The design consists of four functional 'multiplier units', and four associated 'add/subtract units' with registers to accumulate the totals. There is also a 'control unit', implemented as a state machine, to multiplex inputs to different functional units, and also control whether the add/subtract units add or subtract. The meaning of the A, B, C and D signal can be found by careful examination of equations (9) to (12). The apparently complex equations follow a pattern. In particular, it can be noted that there are four distinct sets of operands for the multiplication operations. These four sets, which have been labelled A, B, C and D are shown in Table 2.

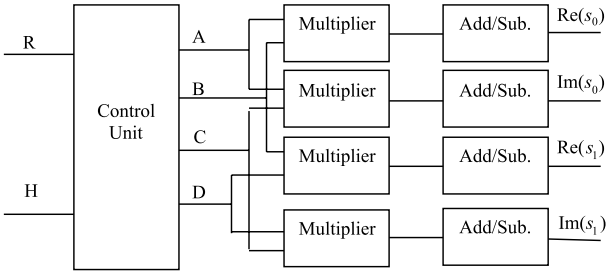

Fig. 3: Block diagram of hardware design of MIMO decoder

Table 2: Sets of operand outputs from control unit

Set	First use	Second use
A	Operand 1 in equation (9)	Operand 1 in equation (10)
B	Operand 2 in equation (9)	Operand 2 in equation (11)
C	Operand 2 in equation (10)	Operand 2 in equation (12)
D	Operand 1 in equation (11)	Operand 1 in equation (12)

To further explain the meaning of Table 2, consider set A as an example. The first usage of A is listed as 'Operand 1 in equation (9)' and the second is 'Operand 1 in equation (10)'. Note, in particular, the first (left hand) operand of any multiplication in equation (9) is the same as the first oper-

and of the corresponding multiplication in equation (10). Because these operands are always the same they are grouped together as set A. Table 2 similarly specifies the members of the other sets. These grouping can be verified by checking them against equations (9) to (12).

It can be seen that the design calculates all the equations for the symbol estimates in parallel. There is one multiplier and one add/subtract unit for each equation being implemented. By exploiting these pairings the control unit is able to multiplex the required inputs through to all of the multiplier functional units using only four multiplexers instead of the eight that would otherwise be required.

4. Hardware Implementation

MIMO testbed development process on FPGA starting from system specification is outlined in Fig. 4. The testbed is first examined with a high level simulation using MATLAB 7.0. Different sub-blocks of the system are then translated for hardware implementation. The HDL used in this work is VHDL for its flexibility of coding styles and suitability for handling very large and complex designs. Xilinx ISE 10.1i and XST engine are used for VHDL synthesis and place-and-route, while Mentor ModelSim XE III 6.3c is used to run functional and post place-and-route simulations. After compilation, simulation and synthesis, configuration files are generated which are used to configure FPGA device. In every step the outputs are verified by comparing with MATLAB simulation result.

The MIMO testbed is implemented on a Xilinx Virtex™-4 LX MB Development Kit. The board included with this kit has a Xilinx XC4VLX60 FPGA device, programmable clock source (25-700 MHz), on-board 100MHz oscillator, a configuration device and access to all of the device signals through available connectors. With all these features the device can be configured to implement very complex systems. Hardware specification for the design of the MIMO realization is listed in Table 3.

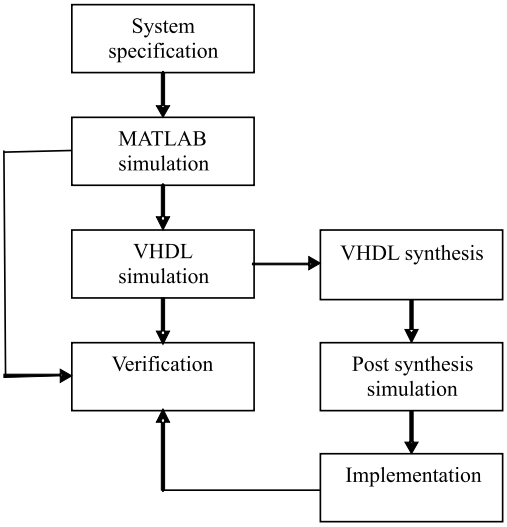

Fig. 4: Design steps of FPGA implementation

Table 3: Hardware Specification of the FPGA Board

FPGA family	Virtex-4
Device	Xilinx XC4VLX60
Programmable clock	25-700 MHz
On-board oscillator	100MHz
Memory	64MB of DDR SDRAM, 4MB of Flash
Logic elements	59,904

The Alamouti scheme based MIMO transmitter contains sequential logic and thus requires some control logic and a clock signal. Fig. 5 shows the schematic of a two transmitter Alamouti encoder implemented using Xilinx® ISE 10.1i. At any symbol period two input bits are modulated by two BPSK modulators. This outputs the real and imaginary components and these are inserted to the Alamouti encoder which encodes the symbols as described above.

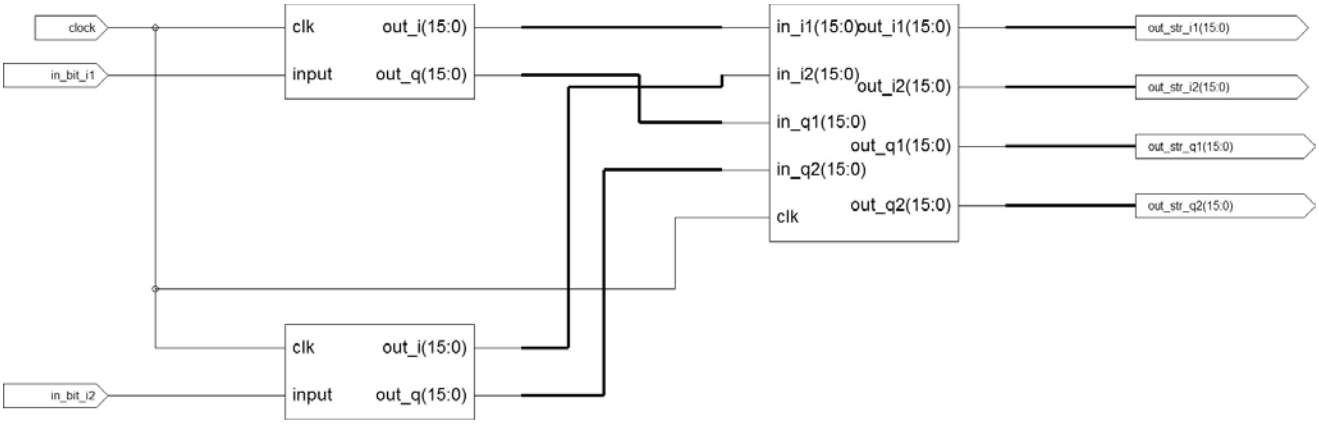

Fig. 5: Schematic of MIMO transmitter

The only operation that the Alamouti encoder performs on modulated symbols is the negation of either the real or imaginary part of a symbol. System clock is used to ensure that all signals are latched at the correct instant of time. It is designed to operate at the same clock speed as the data rate of the system, so one clock cycle is assumed to be one symbol period.

Since it takes two clock cycles to encode two symbols the encoder maintains a 'state' signal to indicate if it is currently the first or second symbol period. This 'state' signal is implemented as a single bit signal that is toggled each clock cycle. The 'state' signal indicates first symbol period when it is 1 and second symbol period when 0. The two BPSK modulated input symbols 'in_i1' and 'in_i2' are encoded to 'out_i1' and 'out_i2' according to Alamouti scheme in two consecutive symbol periods. Fig. 6 presents the FPGA implementation result of Alamouti encoder.

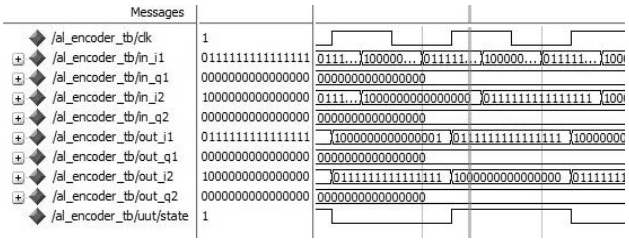

Fig. 6: Simulation result of MIMO encoder

The task of the decoder is to combine the signals simultaneously received in all antennas to construct an improved signal, from which the transmitted signal can be recovered. The MIMO decoder at the receiver takes the input of four 16 bit real and imaginary parts of the channel estimate and four 16 bit real and imaginary parts of the received signals. The design is a multi-cycle implementation; it takes multiple clock cycles to compute the results. The multipliers take one clock cycle to calculate a product and the add/subtract units also take one clock cycle. Therefore two symbol estimates (real and imaginary parts) are produced every 8 clock cycles. The 'done' signal points the end of this 8 clock cycles. A 'reset' signal is also used to reset the decoder. Because of the pairing of the operands as mentioned in Table 3.2, the control logic is able to multiplex the required inputs through to all of the multiplier functional units using only four multiplexers instead of the eight that would otherwise be required. Fig. 7 presents the top level schematic of the MIMO decoder and Fig. 8 shows the simulation result of the decoder. The simulation results are validated against 'bit accurate' MATLAB outputs. Bit accurate refers to the fact that for a given set of input bits the MATLAB simulation will produce the correct output bits.

The MIMO encoder and decoder designs are successfully synthesized using XST engine and then placed and routed on the targeted FPGA. Table 4 shows the device utilization summery of the implementation. This utilization should be considered as an upper bound as there exists a variety of possible optimizations not yet applied to the design.

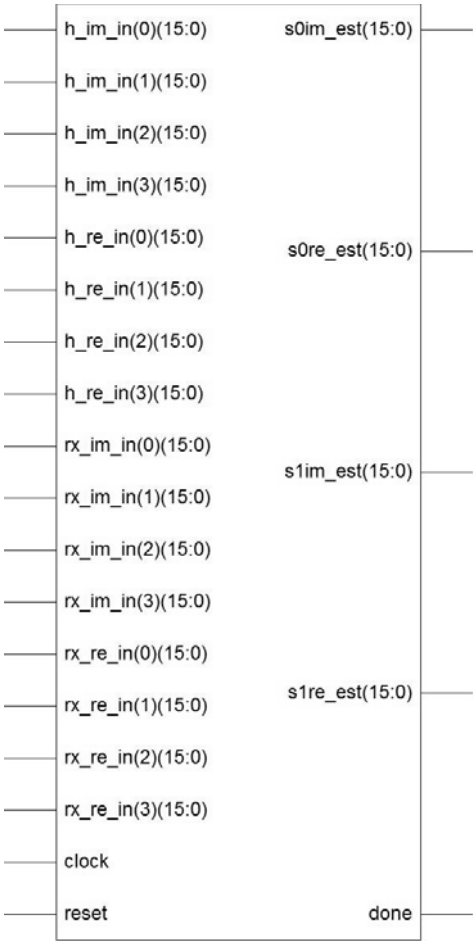

Fig. 7: Top level schematic of MIMO decoder

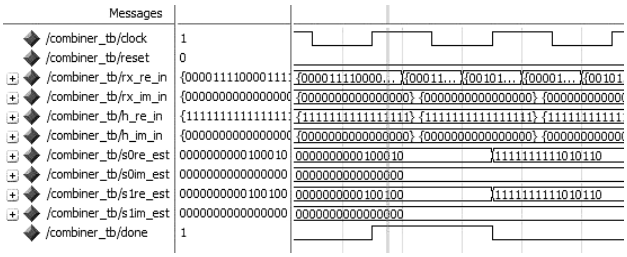

Fig. 8: Simulation result of MIMO decoder

Table 4: Device Utilization Summary

	Available Resources	Used by MIMO Encoder	Used by MIMO Decoder
Slices	26,624	6	393
Slice Flip-flops	53,248	10	355
LUTs	53,248	6	472
Pins	448	67	323

5. Conclusion

4G wireless systems employ multiple antenna techniques to provide high performance while maximizing spectral ef-

ficiency. This prevalence of MIMO systems highlights the need for designed platforms to evaluate such algorithms under realistic conditions. In this paper, the design methodology and implementation of a MIMO testbed is presented, which involves FPGA for fast parallel processing. Main emphasis is led on the ability to extend the hardware in an easy way if the system requires hardware update. The encoder and decoder can be used as standalone units in a single FPGA, or as an element of a complete communication system. The flexibility and wide range of resources of FPGA can thus be very efficient for embedded hardware implementations of future generations of wireless communications systems.

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