A NOVEL CMOS DEFUZZIFICATION CIRCUIT EMPLOYING CURRENT DIFFERENCING BUFFERED AMPLIFIER BASED CURRENT-MODE MULTIPLIERS

Mahmut TOKMAKÇI

Erciyes University, Engineering Faculty, Biomedical Engineering Dept., Kayseri, Turkey

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Abstract: In this paper, design and analysis of a novel current-mode defuzzification circuit is presented. The proposed defuzzification circuit is based on current-mode four-quadrant multipliers that have been constructed with simple current squarer and current differencing buffered amplifier (CDBA). This circuit has capable of high linearity, simple structure, and wide input current range. The defuzzification circuit has been simulated and verified by PSPICE with MIETEC 1.2 μm parameters. The circuit is suitable for using Centre Of Gravity (COG) method in current-mode fuzzy logic controllers. The purpose of this paper is to present an alternative approach for current-mode defuzzification circuit design.

1. Introduction

The defuzzification circuit or defuzzifier is one of the most important units in the fuzzy logic controllers (FLC). There are two ways to implement a defuzzifier: the analogue approach and the digital approach. The analogue approach presents several advantages in front of digital ones, especially regarding speed of processing, power dissipation, and functional density. Moreover, the analogue circuit based fuzzy blocks perform continuous-time processing and they have the particularly to be well compatible with sensors, actuators and all other analogue signals /1-3/. On the other hand, digital circuits are superior to analogue counterpart in accuracy, extendibility, and easy of design automation /4-5/.

Recently, a new five-terminal active current-mode element, called a current differencing buffered amplifier (CDBA), has received much attention in the electronics community /10-12/. It can be operated in both current-mode and voltage-mode in a wide frequency range and can also be implemented with CMOS technology. Differential nature of this element at the input makes it especially suitable for various analogue signal-processing applications demanding high speed, high bandwidth and simple implementation.

In this paper, a new defuzzification circuit employing CDBA based current-mode multipliers is presented. The proposed circuit is built using current-mode four-quadrant multiplier includes simple current squarer and CDBA, and current-mode reverse function circuit as divider unit.

The centre of gravity (COG) is the most popular defuzzification method in FLC. Various defuzzification circuits using COG method are described in literature /6-9/. A high-speed digital defuzzification circuit based on BiCMOS technology has been proposed in /7/ but the fabrication cost is high. The other defuzzification circuit design with current-mode analogue circuits was proposed in /8/. However, both frequency range and speed of these circuits are low. Another defuzzification circuit using resonant tunneling diodes is proposed by Tang and Lin /9/. Their design reduces circuit complexity compared with conventional digital and analogue signal processing circuits.
2. Circuit Description

The COG method in current-mode is expressed as

\[ I_{\text{out}}(\text{COG}) = \frac{\sum_{i=1}^{n} I_{\mu_i} \cdot I_{c_i}}{\sum_{i=1}^{n} I_{\mu_i}} \]  

where \( n \) represents the number of fuzzy sets on the universe of discourse, \( I_{\mu_i} \) and \( I_{c_i} \) represent the membership function output and support value of the \( i \)th fuzzy set, respectively. Eq. (1) can be arranged with current values of input/output variables as follows.

\[ I_{\text{out}} = \frac{I_{\mu_1} \cdot I_{c_1}}{I_{\Sigma}} + \frac{I_{\mu_2} \cdot I_{c_2}}{I_{\Sigma}} + \ldots + \frac{I_{\mu_m} \cdot I_{c_m}}{I_{\Sigma}} \]  

where \( I_{\Sigma} \) is equal to \( \sum_{i=1}^{n} I_{\mu_i} \)

The input and the output characteristics of each term in equation (2) can be defined by using current-mode four-quadrant multiplier blocks. Each block in Eq. (2) is computed as follows:

\[ I_{\text{out}} = \frac{I_x \cdot I_y}{I_w} \]

(3)

where \( I_x, I_y, I_w \) and \( I_{\mu}, I_{c}, I, I_{\mu'} \) variables are corresponded with \( I_{\mu_i}, I_{c_i}, I \), and \( I_{\mu_{i'}} \), respectively. The block diagram of defuzzification circuit processing unit in Eq. (3) is implemented with two multipliers and one current-mode reverse function block as shown in Fig.1.

Fig. 1: The block diagram of defuzzification circuit processing unit

The building blocks of current-mode multiplier circuit are shown in Fig. 2. This multiplier circuit is consists of two cascode current mirrors, one modified current differencing amplifier (CDBA), and three current squarer units.

The modified circuit structure of the CDBA in /10/ and circuit symbol is shown in Fig. 3 (a) and (b), respectively. The characteristic equation of this element can be given as

\[ V_p = V_n = 0, \quad I_z = I_p - I_n, \quad V_w = V_z \]  

(4)

Here, current through z-terminal follows the difference of the current through p-terminal and n-terminal. Input terminals, p and n, are internally grounded. A possible CMOS realization of CDBA consisting of a differential current

controlled current source (DCCCS) followed by a voltage buffer is shown in Fig. 3 (a).

2.1. Current Squarer

The current squarer circuit into four-quadrant multiplier is shown in Fig. 4. The MOSFETs, M1, M2, and M3, are the identical transistors, working in saturation region. In condition that \( V_{gs} > V_g \) and \( V_{gs} > V_{gd} - V_g \), the expression of drain current for the simple MOS transistor operating in saturation region is

\[ I_{ds} = \mu C_{ox} \left( \frac{W}{L} \right) (V_{gs} - V_T)^2 \]  

(5)

\[ I_{ds} = K (V_{gs} - V_T)^2 \]  

(6)

Where \( K \) is trans-conductance parameter, and \( \mu, C_{ox}, W \), and \( L \) stand for carrier effective mobility, gate oxide capacitance per unit area, width, and length of the channel, respectively /13/.

In Fig. 4, \( V_g \) and \( I_{ds} \) are the dc bias voltage and input current, respectively. If all MOS transistors operate in saturation
If KCL is applied to A and B nodes, output current $I_{out}$ can be obtained as follows:

$$I_{out} = I_{d1} + I_{d3}$$  \hspace{1cm} (8)

Using equations (4)-(5), $I_{out}$ can be derived as follows

$$I_{out} = 2I_{d1} + I_{in}$$  \hspace{1cm} (10)

The voltage of node A, $V_A$, is equal to $V_{gs2}$ and the drain current of $M_1$ transistor can be obtained by using equation (1) and (2).

$$V_A = V_{gs2} = \sqrt{\frac{I_{in} + I_{d1}}{K}} + V_t$$  \hspace{1cm} (11)

$$I_{d1} = K[V_B - V_{gs2} - V_t]^2$$  \hspace{1cm} (12)

Using equation (7) into (8), the drain current of $M_1$, transistor, $I_{d1}$, can be obtained as follows:

$$I_{d1} = \frac{I_{in}}{4K(V_B - 2V_t)^2} + \frac{K}{4}(V_B - 2V_t)^2 - \frac{I_{in}}{2}$$  \hspace{1cm} (13)

If equation (9) is placed into equation (6), the output current $I_{out}$ is given by

$$I_{out} = \frac{I_{in}^2}{2K(V_B - 2V_t)^2} + \frac{K}{2}(V_B - 2V_t)^2$$  \hspace{1cm} (14)

Here, $K$ is the transconductance parameter, $V_B$, and threshold voltage, $V_t$, are constant values and are chosen by designers.

Figure 5 shows current-mode reverse function (1/x or $x^{-1}$) circuit as divider operator in proposed defuzzification unit. This circuit is basically current square/divider circuit. The reverse function circuit output current $I_{out}$ is obviously given by

$$I_{out} = \frac{I_{bias}}{4I_w}$$  \hspace{1cm} (16)

$$I_{out} = \frac{A}{I_w} \quad \text{for} \quad A = \frac{I_{bias}}{4}$$  \hspace{1cm} (17)

Here, $I_{bias}$ is corresponded to squaring current and it has been fixed value as dividing coefficient, i.e. $A = \frac{I_{bias}}{4}$. Thus, the circuit can be converted to divider operator by fixing squaring current $I_{bias}$. In this circuit, the voltage-translinear loops are formed by transistors $M_1$-$M_{10}$; note that the bulk terminals of these transistors are connected to their sources, thus avoiding the body effect. $M_{13}$ and $M_{26}$ are diode-connected transistors included for decreasing the channel-length modulation effect in $M_1$ and $M_2$, respectively. Transistors $M_{11}$-$M_{12}$ form a current mirror and $M_{14}$-$M_{25}$ constitute high-swing cascode current copiers employed for injecting the required combinations of currents into the voltage-translinear loop. The circuit is designed for $VDD = 2.5 \, V$ and $V_C = 1.3 \, V / 14/.

### 3. Simulation Results

The behaviour of the implemented CDBA and simple current squarer based defuzzification circuit was confirmed with 1.2 μm MIETEC CMOS process parameters by PSPICE simulations. The all device dimensions of the squarer circuit in Fig. 4 are identical and W/L= 120 μm/2 μm. The transient analysis results of current-mode reverse function circuit are shown in Fig. 6. Here, $I_{bias}$ current is corresponded to
input current range and high frequency features of proposed circuit because of using CDBA structure in current-mode four-quadrant multipliers. In the simulations of proposed defuzzification circuit, the circuit parameter values are determined as follows: $V_{DD} = -V_{SS} = 2.5 \text{ V}$, $-200 \mu\text{A} \leq I_y (I_{in}) \leq +200 \mu\text{A}$, $-15 \mu\text{A} \leq I_x (I_{\mu i}) \leq 15 \mu\text{A}$, $V_b1 = -1.45 \text{ V}$, $R_L = 1 \text{ K}\Omega$.

The mathematical and simulation results of defuzzification processing unit are shown together in Fig. 8. Three input sinusoidal signals $(I_x, I_y, I_w)$ are applied defuzzification processing unit. The simulation result of defuzzification circuit is verified to calculation result as shown in Fig. 8.

4. Conclusions

A novel current-mode defuzzification circuit using Centre of Gravity (COG) method has been designed and analyzed. Its behaviour was confirmed by PSPICE simulation experiments with MIETEC 1.2 μm CMOS process. The implemented defuzzification circuit is based on current-mode four-quadrant multipliers and modified current squarer/divider circuits as divider operator in defuzzification processing unit. The proposed current-mode defuzzification circuit has capable of high linearity, simple structure, and wide input current range. The features are verified with PSPICE simulation experiments. The defuzzification circuit is suitable for CMOS fuzzy logic controllers with Centre Of Gravity (COG) method.

References


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Mahmut TOKMAKÇI
Erciyes University, Engineering Faculty, Biomedical Engineering Dept., 38039, Kayseri, Turkey
E-mail: tokmakci@erciyes.edu.tr

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