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Modeling and Simulation of High Level Leakage Power Reduction Techniques for 7T SRAM Cell Design

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Abstract: In this paper, the process of 7T SRAM cell is analyzing and also exploring the circuit topologies, high level leakage power reduction techniques and cell parameters. The first segment contains the information about process of the 7T SRAM cell like write operation and read operation. Second segment of this paper characterize high level the leakage power reduction techniques, containing the information about how many types of techniques are available for characterizing the high level leakage power reduction techniques and what is the effect on the high level leakage power reduction techniques on 7T SRAM cell design. The third segment of this paper shows the information about cell parameters means how many parameters we use to describe our circuit. This segment of the paper is the most important segment because this segment contains the information about all the parameters of 7T SRAM cell. In the second segment of this paper contains the information about high level leakage power reduction techniques, by using high level leakage power reduction techniques we can make our 7T SRAM cell much better in different area like power dissipation, leakage power reduction, short circuit power consumption, dynamic power consumption, cell write delay, cell read delay, static noise margin. The data of leakage power consumption shows that after voltage scaling technique leakage power consumption and dynamic power consumption is less.

Keywords: 7T SRAM cell, leakage power reduction, short circuit power consumption, dynamic power consumption, static power consumption, cell write delay, cell read delay, static noise margin.

Modeliranje in simulacije tehnik znižanja visoke stopnje izgub v 7T SRAM celici

Izvleček: Članek opisuje analizo 7T SRAM celice in raziskuje topologije vezja, tehnike znižanja visoke stopnje izgub in parametre celice. V prvem delu je predstavljeno delovanje 7T SRAM celice v smislu operacije pisanja in branja. V drugem delu so karakterizirane tehnike izgub in kakšen vpliv imajo na dizajn celice. V tretjem delu so opisani vsi parametri, ki jih potrebujemo za opis vezja celice. Podatki izgub pokažejo, da so, pri uporabi tehnike skaliranja napetosti, izgube manjše.
Ključne besede: 7T SRAM celica, znižanje izgub, poraba kratkostičnega vezja, dinamična poraba energije, statična poraba energije, zakasnitve pri pisanju in branju, meje statičnega šuma

Ključne besede: 7T SRAM celica, znižanje izgub, poraba kratkostičnega vezja, dinamična poraba energije, statična poraba energije, zakasnitve pri pisanju in branju, meje statičnega šuma

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1. Introduction

In this paper, the process of 7T SRAM cell is analyzing and also exploring the circuit topologies, high level leakage power reduction techniques and cell parameters. In the first segment 7T SRAM cell, describing circuit topologies means how to make our circuit, which type of component used to make our circuit, what are the properties of the component by which we will make our circuit? The second segment contains the information about process of the 7T SRAM cell like write operation and read operation. Third segment of this paper characterize high level the leakage power reduction techniques, containing the information about

how many types of techniques are available for characterizing the high level leakage power reduction techniques and what is the effect on the high level leakage power reduction techniques on 7T SRAM cell design. The fourth segment of this paper shows the information about cell parameters means how many parameters we use to describe our circuit. This segment of the paper is the most important segment because this segment contains the information about all the parameters of 7T SRAM cell. In the third segment of this paper contains the information about high level leakage power reduction techniques, by using high level leakage power reduction techniques we can make our 7T SRAM cell much better in different area like power dissipation, leakage power reduction, short circuit power consumption, dynamic power consumption, cell write delay, cell read delay, static noise margin.

2. Process topology

In this segment we will study about various types of 7T SRAM cell's process[1, 2] like how to write in a 7T SRAM cell to store in the memory. Firstly various types of schematic of the 7T SRAM cell is shows below

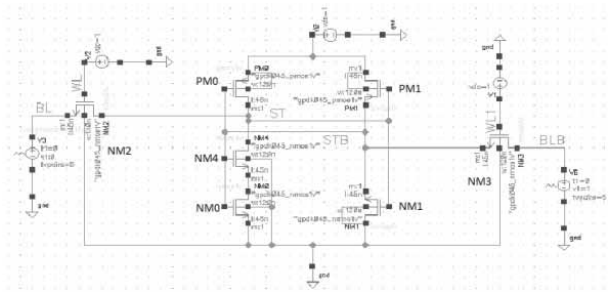

Figure 1: Schematic of 7T1 SRAM cell

This figure shows the schematic of 7T1 SRAM cell, in this circuit seven transistor uses to make the circuit. For making the circuit we use two PMOS which named as PMO and PM1 and five NMOS which named as NMO, NM1, NM2, NM3 and NM4. NM2 and NM3 are called as access transistor and source of the NM2 and NM3 are connected by the BL and BLB respectively and gate of the NM2 and NM3 are connected by the WL and WL1 respectively. The second schematic shows below for 7T2 SRAM cell

This figure shows the schematic of 7T2 SRAM cell, in this circuit seven transistor uses to make the circuit. For making the circuit we use two PMOS which named as PMO and PM1 and five NMOS which named as NMO, NM1, NM2, NM3 and NM4. NM2 and NM3 are called as access transistor and source of the NM2 and NM3 are connected by the BL and BLB respectively and gate of

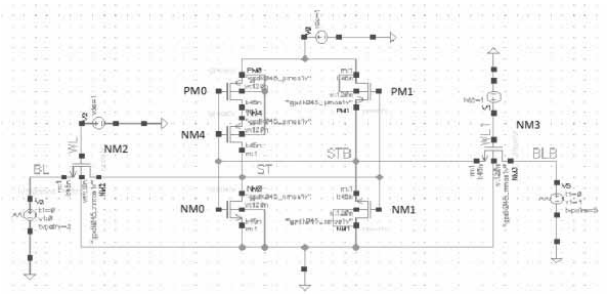

Figure 2: Schematic of 7T2 SRAM cell

the NM2 and NM3 are connected by the WL and WL1 respectively.

The third schematic shows below for 7T3 SRAM cell

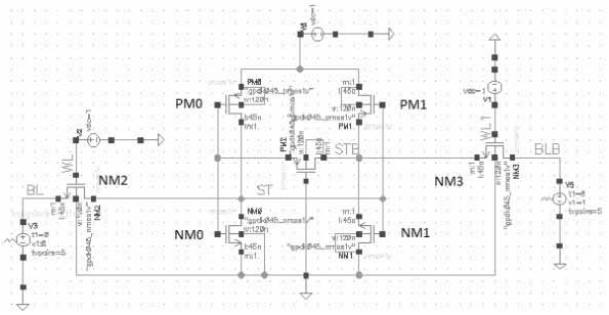

Figure 3: Schematic of 7T3 SRAM cell

This figure shows the schematic of 7T3 SRAM cell, in this circuit seven transistor uses to make the circuit. For making the circuit we use two PMOS which named as PMO and PM1 and five NMOS which named as NMO, NM1, NM2, NM3 and NM4. NM2 and NM3 are called as access transistor and source of the NM2 and NM3 are connected by the BL and BLB respectively and gate of the NM2 and NM3 are connected by the WL and WL1 respectively.

2.1 Write operation

Write operation of various 7T SRAM cell are same for all the 7T SRAM cells. It is started from the NM2 and NM3 transistor because the source of the NM2 and NM3 are working as an input for a write operation. After giving input to the BL and BLB as a VDD and GND respectively and making the WL and WL1 at VDD level, the data goes to the SRAM cell and store at the ST and STB node. The value of the ST and STB node will be opposite means "1V(VDD)" and "0V(GND)" respectively.

The write analysis of the various 7T SRAM cell is shown in the table below

Table 1: Write analysis of the various 7T SRAM cell

S. No	Values	SRAM cell					
		7T1		7T2		7T3	
		1.5 ns	3.5 ns	1.5 ns	3.5 ns	1.5 ns	3.5 ns
1	BL	1V	0V	1V	0V	1V	0V
2	BLB	0V	1V	0V	1V	0V	1V
3	ST	1V	20.66 nV	1V	352 nV	1V	1.4 uV
4	STB	0.6 uV	1V	396 nV	1V	57 uV	1V

2.2 Read operation

The read operation of SRAM cell started from the transistor known as NM2 and NM3 because from these transistors we can either write or read and at this time we will use these transistors as a read transistor. At this point from the source end of the NM2 and NM3 transistor in which BL and BLB connected we will use as a output node.

The write analysis of the various 7T SRAM cell is shown in the table below

Table 2: Read analysis of the various 7T SRAM cell

S. No	Values	SRAM cell					
		7T1		7T2		7T3	
		1.5 ns	3.5 ns	1.5 ns	3.5 ns	1.5 ns	3.5 ns
1	BL	1V	0V	1V	0V	1V	0V
2	BLB	0V	1V	0V	1V	0V	1V
3	ST	1V	186 nV	1V	27 nV	1V	653 mV
4	STB	1.3 uV	1V	42 nV	1V	38 nV	376 mV

3. Leakage power reduction techniques

There are several techniques available for reduction of the leakage power. But here we discuss about only one technique which name is voltage scaling.

3.1 Voltage scaling

Reducing the power supply voltage is the effective technique to reduce static power leakage and the write delay. Keeping all others factors constant if power scaling is scaled down propagation delay will increase. This can be compensated by scaling down the threshold voltage to the same extent as the supply voltage. This allows the circuit to produce the same speed performance at a lower Vdd. At the same time smaller threshold voltages lead to smaller noise margin and increased leakage current.

3.1.1 Write operation after voltage scaling techniques

Write operation of various 7T SRAM cell are same for all the 7T SRAM cells. It is started from the NM2 and NM3 transistor because the source of the NM2 and NM3 are working as an input for a write operation. After giving input to the BL and BLB as a VDD and GND respectively and making the WL and WL1 at VDD level, the data goes to the SRAM cell and store at the ST and STB node. The value of the ST and STB node will be opposite means "1V(VDD)" and "0V(GND)" respectively.

The write analysis of the various 7T SRAM cell after voltage scaling technique is shown in the table below

Table 3: Write analysis of the various 7T SRAM cell after voltage scaling technique

S. No	Values	SRAM cell					
		7T1		7T2		7T3	
		1.5 ns	3.5 ns	1.5 ns	3.5 ns	1.5 ns	3.5 ns
1	BL	0.7V	0V	0.7V	0V	0.7V	0V
2	BLB	0V	0.7V	0V	0.7V	0V	0.7V
3	ST	0.7V	97.43 nV	0.7V	182 nV	329 mV	65.37 nV
4	STB	179 nV	0.7V	532 nV	0.7V	1.4 mV	0.7V

3.1.2 Read operation after voltage scaling techniques

The read operation of SRAM cell started from the transistors known as NM2 and NM3 because from these transistors we can either write or read and at this time we will use these transistors as a read transistor. At this point from the source end of the NM2 and NM3 transistor in which BL and BLB connected we will use as a output node.

The write analysis of the various 7T SRAM cell after voltage scaling technique is shown in the table below

Table 4: Read analysis of the various 7T SRAM cell after voltage scaling technique

S. No	Values	SRAM cell					
		7T1		7T2		7T3	
		1.5 ns	3.5 ns	1.5 ns	3.5 ns	1.5 ns	3.5 ns
1	BL	0.7V	0V	0.7V	0V	0.7V	0V
2	BLB	0V	0.7V	0V	0.7V	0V	0.7V
3	ST	0.7V	77.4 nV	0.7V	83 nV	378 mV	155.4 mV
4	STB	100.5 nV	0.7V	32 nV	0.7V	3.5 nV	0.7 mV

4. Circuit parameters

In this segment of the paper all the parameters described which is related to the 7T SRAM cell design. There are various parameters uses to describe the circuit like short circuit power consumption, dynamic power consumption, static power consumption, cell write delay, cell read delay, static noise margin. But we will discuss about leakage power consumption.

4.1 Leakage power consumption

While the CMOS inverter is in stable state[3], it has either its p- or n- MOS transistor shot off. In an ideal world there would be no current flowing from the power supply to the ground. However there is a small leakage current flowing through the shot off transistor giving rise to leakage power consumption, specified by formula 1.

$$P = I\,leak \times V\,dd \tag{1}$$

By using this formula we can calculate the leakage power consumption for various 7T SRAM cells. After calculating the leakage power consumption we will use the leakage power reduction technique which name is voltage scaling technique and after that we will again calculate the leakage power consumption for the various 7T SRAM cell. This Leakage power consumption is shown in table below

Table 5: Leakage Power Consumption for Various 7T SRAM cells

S. No	SRAM	Leakage Power Consumption			
		Before Voltage Scaling		After Voltage Scaling	
		ST node	STB node	ST node	STB node
1	7T1	0.76 nW	0.97 nW	0.71 nW	0.88 nW
2	7T2	0.66 nW	0.82 7nW	0.51 nW	0.68 nW
3	7T3	0.92 nW	0.58 nW	0.76 nW	0.43 nW

For 7T1 SRAM cell after using the voltage scaling technique we characterize that for the ST node leakage power consumption is 6.57% less with respect to before using voltage scaling technique and for the STB node leakage power consumption is 9.27% less with respect to before using voltage scaling technique. For 7T2 SRAM cell after using the voltage scaling technique we characterize that for the ST node leakage power consumption is 22.72% less with respect to before using voltage scaling technique and for the STB node leakage power consumption is 17.07% less with respect to before using voltage scaling technique. For 7T3 SRAM cell after using the voltage scaling technique we characterize that for the ST node leakage power consumption is 17.39% less with respect to before using voltage scaling technique and for the STB node leakage power consumption is 25.86% less with respect to before using voltage scaling technique.

4.2. Dynamic power consumption

When the CMOS inverter switches from one state to another the output capacitor CL have to be either charged or discharged[4, 5]. Energy is consumed and transformed to heat in the MOS transistors. The energy consumed is equal to the energy needed to charge CL. The energy is specified according to formula 2.

$$E = V_{dd} * Q = V_{dd} * C_L * V_{swing} \tag{2}$$

Vdd is the power supply voltage and V_{swing} the voltage swing on the output of the inverter. If the V_{swing} is the same as Vdd, which is common, the energy becomes,

$$E = C_L * V_{dd} \tag{3}$$

The dynamic power consumption is the energy drawn from the power supply during one second. The power consumed is calculated as in formula 4, where f is the switching frequency.

$$P = ½ * f * C_L * V_{dd}^2 \quad (4)$$

CL is only charged at transition from low to high (zero to Vdd), therefore the division by 2. In a general case, f symbolizes the clock frequency. In this case the constant α is added to express the switching activity as in formula 5.

$$P = ½ * \alpha * f * C_L * V_{dd}^2 \quad (5)$$

By using these formulas we can calculate the dynamic power consumption for various 7T SRAM cells. After calculating the dynamic power consumption we will use the dynamic power reduction technique which name is voltage scaling technique and after that we will again calculate the dynamic power consumption for the various 7T SRAM cell. This dynamic power consumption is shown in table below

Table 6: Leakage Power Consumption for Various 7T SRAM cells

S. No	SRAM	Leakage Power Consumption			
		Before Voltage Scaling		After Voltage Scaling	
		ST node	STB node	ST node	STB node
1	7T1	0.66 nW	0.86 nW	0.53 nW	0.81 nW
2	7T2	0.43 nW	0.74 7nW	0.38 nW	0.65 nW
3	7T3	0.79 nW	0.78 nW	0.71 nW	0.65 nW

For 7T1 SRAM cell after using the voltage scaling technique we characterize that for the ST node dynamic power consumption is 19.69% less with respect to before using voltage scaling technique and for the STB node dynamic power consumption is 5.81% less with respect to before using voltage scaling technique. For 7T2 SRAM cell after using the voltage scaling technique we characterize that for the ST node dynamic power consumption is 11.62% less with respect to before using voltage scaling technique and for the STB node dynamic power consumption is 12.16% less with respect to before using voltage scaling technique. For 7T3 SRAM cell after using the voltage scaling technique we characterize that for the ST node dynamic power consumption is 10.12% less with respect to before using voltage scaling technique and for the STB node dynamic power consumption is 16.66% less with respect to before using voltage scaling technique.

5. Conclusion

The conclusion of the paper explain that after using the leakage power reduction technique which name is voltage scaling the waveform of write operation and read operation is quite different from the initial one. The average leakage power consumption after using voltage scaling technique is 7.92% less from the initial one for 7T1 SRAM cell. The average leakage power consumption after using voltage scaling technique is 19.895% less from the initial one for 7T2 SRAM cell. The average leakage power consumption after using voltage scaling technique is 21.625% less from the initial one for 7T3 SRAM cell. In the next segment of the conclusion the major thing is dynamic power consumption. The average dynamic power consumption after voltage scaling for the 7T1 SRAM cell is 12.75% less than the initial one. The average dynamic power consumption after voltage scaling for the 7T2 SRAM cell is 11.89% less than the initial one. The average dynamic power consumption after voltage scaling for the 7T3 SRAM cell is 13.39% less than the initial one. The whole process for calculating the leakage power and dynamic power after using voltage scaling technique is perform better than the initial one.

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