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Effects of static and pulsed negative bias temperature stressing on lifetime in p-channel power VDMOSFETs

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Abstract: Threshold voltage shifts associated with negative gate bias temperature instability in p-channel power VDMOSFETs under the static and pulsed stress conditions are analysed in terms of the effects on device lifetime. The pulsed bias stressing is found to cause less significant threshold voltage shifts in comparison with those caused by the static stressing, which is ascribed to the effects of dynamic recovery and shorter actual stress time associated with pulsed bias conditions. Accordingly, pulsed gate bias conditions provide much longer device lifetime than the static ones, which is shown by individual use of the $1/V_G$ and 1/T models for extrapolation to normal operation voltage and temperature, respectively, as well as by combined use of both models for a double extrapolation successively along both voltage and temperature axes. A double extrapolation approach is shown to allow for construction of the surface area representing the lifetime values corresponding to a full range of device operating voltages and temperatures.

Key words: Lifetime estimation, NBTI, VDMOSFET

Vpliv statičnega in pulznega negativnega temperaturnega stresa na življenjske čase v kanalu p močnostnih VDMOSFET-ov

Povzetek: Premik pragovne napetosti zaradi negativne nestabilnosti vrat v kanalu p močnostnih VDMOSFETov v statičnih in pulzno vzbujanih pogojih so analizirani v smislu vplivov na življenjske čase elementa. Izkazalo se je, da pulzno vzbujanje povzroča manjše premike pragovne napetosti glede na razmere pri statičnem vzbujanju, kar lahko pripisujemo vplivom dinamičnega okrevanja in kratkim dejanskim časom pulznega vzbujanja. Pulzno vzbujanje omogoča precej daljše življenjske čase kot pri statičnih pogojih, kar se izkazuje pri individualni uporabi $1/V_G$ in 1/T modelov za ekstrapolacijo do normalnih napetosti in temperatur obratovanja, kakor tudi pri kombinirani uporabi obeh modelov pri ekstrapolaciji po temperaturni in napetostni osi. Dvojna ekstrapolacija omogoča površinski prikaz življenjskih časov preko celotnega temperaturnega in napetostnega območja delovanja elementa.

Ključne besede: Ocena življenjskih časov, NBTI, VDMOSFET

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1. Introduction

With device dimensions in MOS technologies being continuously scaled down, a phenomenon named negative bias temperature instability (NBTI) has been gaining in importance to become widely recognised as one of the most critical mechanisms of device degradation in state-of-the-art CMOS circuits. NBTI refers to the complex physical mechanisms involving generation of oxide-trapped charge and interface traps in MOS structures exposed to stressing by negative gate bias at elevated temperature, and was found to occur mostly in p-channel MOSFETs operated at elevated temperatures (100-250 °C) under negative gate voltages producing gate oxide electric fields in the range 2-6 MV/cm [1-6]. It leads to serious changes in device threshold voltage and may also reduce the transconductance and drain current. Threshold voltage shifts associated with NBTI

are strongly dependent on the stress parameters (gate voltage, temperature, time) and are particularly critical for reliable operation and lifetime of p-channel devices with thin gate oxides [2-4]. However, NBTI could be also critical for reliability of ultra-thick gate oxide devices, such as power MOSFETs. Power MOSFETs, widely used as fast switching devices in home appliances and automotive, industrial and military electronics, are routinely operated at high current and voltage levels, which lead to both self-heating and increased gate oxide fields and thus favour NBTI [7, 8].

In spite of extensive studies over the recent years [1-3, 5, 6], microscopic mechanisms of NBTI are still not well understood, so the technology optimization to minimize NBTI is yet to be achieved. Therefore, accurate models and well established procedures for lifetime estimation are required to make good prediction of device reliable operation. There are several commonly used models for extrapolation along the voltage or electric field axis, such as "V_G", "$1/V_G$" and "power-law" models [9, 10], which enable the use of experimental data obtained under the accelerated stress conditions (increased gate voltage and elevated temperature) to estimate device lifetime for normal operation voltage. These models, however, yield the lifetime only for the temperatures applied during the stressing, so an extrapolation along the temperature axis by "1/T" model, which enables estimation of the lifetime at normal operation temperature, has recently also been proposed [11-13]. A double extrapolation, along both voltage and temperature axes, that lead to lifetime estimates for any reasonable combination of operation voltage and temperature, has been proposed as well [11-13].

It is important to note that gate bias applied during operation of MOS devices in a number of applications switches between the "high" and "low" voltage levels, thus creating the pulsed stress conditions. Some earlier investigations of pulsed NBTI have shown that oxide-trapped charge and interface traps generated during application of the "high" gate voltage level are partially neutralized and/or annealed while the gate is at "low" voltage level [14-17]. So, the lifetime predictions based on static NBT stress conditions [18, 19], where the gate was continuously kept at "high" voltage level, could be wrong, and it is thus necessary to estimate device lifetime under the pulsed NBT stress conditions.

Given the above considerations, in this paper the effects of static and pulsed NBT stressing on threshold voltage in commercial p-channel power VDMOSFETs will be compared in terms of device lifetime. The $1/V_G$ and 1/T models will be applied to appropriate data for NBT stress-induced threshold voltage shift for two separate extrapolations along the voltage and temperature axes in order to get lifetime estimates for the voltages and temperatures expected in device normal operation mode. A double successive extrapolation along the voltage and temperature axes, which extends the validity of the above models to any reasonable set of operation voltages and temperatures, and may provide more realistic lifetime prediction in MOS devices operated under the normal conditions, will be demonstrated as well.

2. Experiment

Devices investigated in this study were commercial p-channel power VDMOSFETs IRF9520, built in standard silicon-gate technology with approximately 100 nm thick gate oxide, which were encapsulated in TO-220 plastic packages. They had the initial threshold voltage $V_{T0} = -3.6$ V and current and voltage ratings of 6.8 A and 100 V, respectively. For the static NBT stress, several sets of devices have been stressed up to 48 hours by applying negative dc voltages in the range 35-45 V to the gate, while drain and source terminals were grounded [18-21]. For the pulsed stress, negative gate voltage pulses (typically 10 kHz, 50 % duty cycle) of the same magnitudes were used. As indicated in Fig. 1, term "stress time" for pulsed stressing in this study refers to the total time, including both the net stress time at V_G (time fraction corresponding to a "high" voltage level of pulsed gate bias) and the time at zero gate bias (time fraction corresponding to the "low" voltage level). Stressing under both static and pulsed conditions was performed at temperatures ranging from 125 to 175 °C.

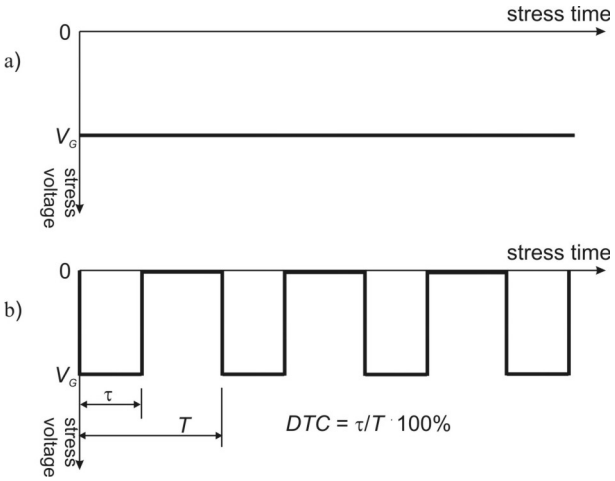

Figure 1: Stress voltage waveforms during the static a) and pulsed b) NBT stress.

Experimental setup for NBT stressing and electrical characterization of stressed devices (measurements of transfer *I-V* characteristics) is illustrated in Fig. 2. As the

accelerated stressing of the above power devices required voltage amplitudes even exceeding 40 V, which were beyond the capabilities of commonly used signal source units [22-24], the inclusion of an external amplifier (booster) between the source unit and the device under test (DUT) was necessary to supply the required stress voltage to DUT. Switches S1 and S2 were used to separate high-voltage stress circuit from the low-voltage measurement circuit (source and drain of DUT were tied to ground during the stress). Gate stress voltage was obtained from the source unit acting either as a dc source or a pulse generator (Tektronix AFG3102), for static and pulsed NBT stress conditions, respectively. Swept gate measurement voltage was provided from the Agilent 6645A source unit, while an Agilent 4156C semiconductor parameter analyzer was used as the source-measure unit for drain biasing and drain current measurements. All the instrumentation, along with the temperature inside the chamber (Heraeus HEP2), have been computer controlled over IEEE-488 GPIB bus.

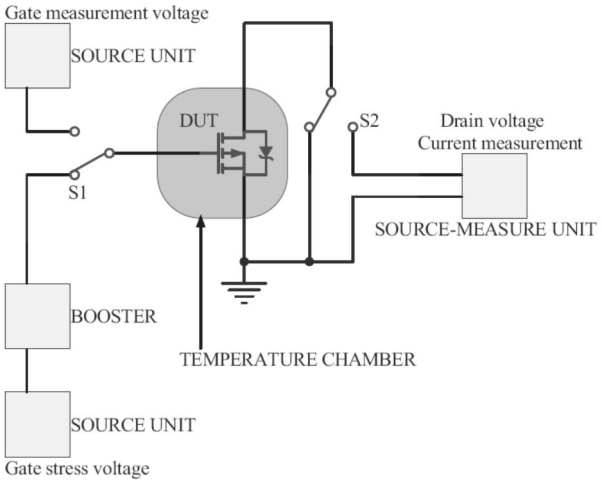

Figure 2: Block diagram for NBT stress and fast measurement on p-channel power VDMOS transistor.

Typical transfer *I-V* characteristics of p-channel power VDMOSFETs measured during the static and pulsed NBT stressing with V_G = – 45 V at 175 °C are shown in Figs. 3 and 4, respectively. It can be seen that, as the stressing progressed, the characteristics were being shifted along the V_{GS} axis towards the higher voltage values, which was the consequence of stress-induced buildup of oxide-trapped charge. The shifts were more significant in the case of static NBT stressing. Also, in both cases the shifts were more pronounced in the early phase of stressing and gradually became smaller in the advanced phase. At the same time, the slope of the transfer characteristics slightly decreased, indicating that interface traps were being generated as well.

Dependencies of stress-induced threshold voltage shifts (ΔV_T) on NBT stress time in devices stressed at several different temperatures with different gate voltages for both static and pulsed stress conditions are shown in Fig. 5. As can be seen, NBT stressing under both static and pulsed gate bias conditions was found to cause significant threshold voltage shifts, which in accordance with observed shifts of transfer characteristics along the voltage axis were more pronounced at higher voltages and/or temperatures. The threshold voltage shifts in the case of pulsed NBT stress appeared with rather significant time delay (30-60 minutes after the start of stressing), which was found to depend on stress temperature and pulse magnitude. In addition, the pulsed stressing caused generally lesser shifts as compared to static stressing performed at the same temperature with the same magnitude of stress voltage. The reason for the observed delay and lesser shifts in the case of pulsed NBT stress can be found in the nature of pulsed stressing itself. As already mentioned, "stress time" in the case of pulsed stress refers to the total time, which includes the time fractions corresponding to both "high" and "low" levels of the pulsed gate voltage applied. Devices are actually stressed only during the time fraction corresponding to a "high" voltage level of pulsed stress voltage, so the actual stress time is significantly shorter than the total time. Also, threshold voltage tends to recover during the time fraction corresponding to a "low" level, and this dynamic recovery of threshold voltage is an additional reason why the resulting shifts appear more slowly and are lower in the case of pulsed NBT stress.

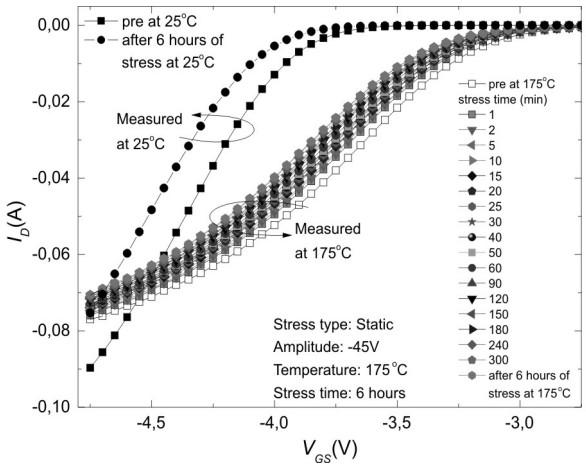

Figure 3: I_D-V_{GS} characteristics of p-channel power VDMOSFETs during the static NBT stressing.

3. NBTI effects on device lifetime

Degradation associated with NBTI can put serious limit to the lifetime of devices operated at elevated temperatures under the increased gate oxide electric field. Our goal in this study was to estimate normal operation lifetime of investigated p-channel power VDMOSFETs

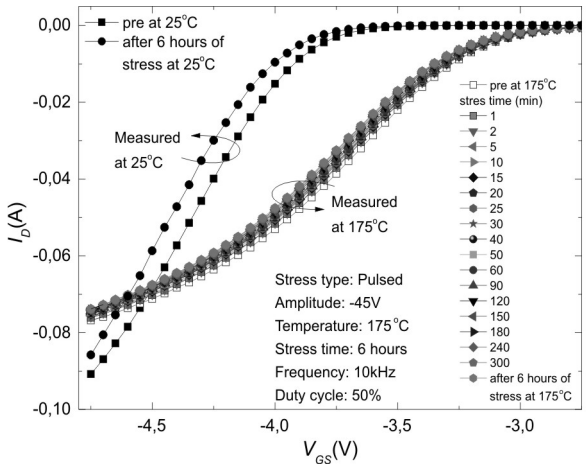

Figure 4: I_D-V_{GS} characteristics of p-channel power VDMOSFETs during the pulsed NBT stressing.

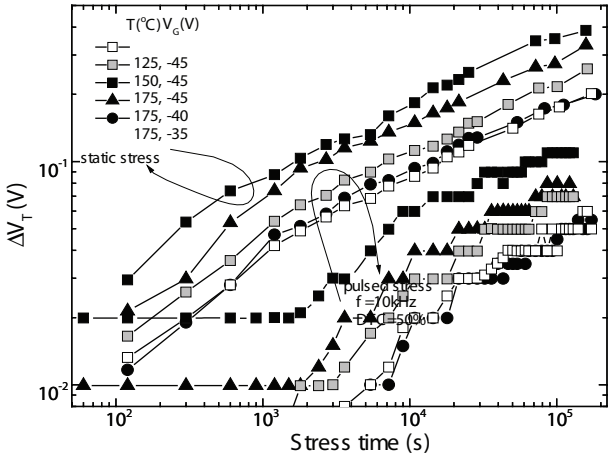

Figure 5: Threshold voltage shifts in p-channel VDMOSFETs during the static and pulsed (f = 10 kHz, DTC=50%) NBT stressing at different voltage magnitudes and temperatures.

by using the experimental data obtained under accelerated NBT stress conditions. Devices under test were the power transistors, so we could assume maximum normal bias V_G = – 20 V and temperature T = 100 °C.

To estimate the device lifetime it is necessary to choose one of device parameters affected by the stress, which would be suitable to monitor the level of stress-induced degradation, as well as to define an appropriate failure criterion (FC) as a maximum allowed change of the chosen parameter that is critical for device and/or circuit reliable operation. Various parameters, such as threshold voltage, transconductance, or drain current, can be used as degradation monitor for the lifetime estimation [25, 26]. Threshold voltage has widely been accepted as a well-suited parameter, so in this study we will use the experimental results for NBT stress-induced threshold voltage shift as degradation monitor to estimate device lifetime in practical operation.

The standard procedure of lifetime estimation requires first to extract the values of lifetime the devices would have if operated under the experimental conditions, and then use these experimental lifetime values for extrapolation to normal operating conditions.

3.1. Extraction of experimental lifetime data

Experimental lifetime is defined as the stress time required for the stress-induced ΔV_T to reach failure criterion, which in our case was set at 50 mV (a proper choice of failure criterion is important, and was discussed in our earlier paper [18]). The extraction of experimental lifetime values from our data, for stressing with different gate voltage magnitudes at T = 150 °C and for stressing with V_G = – 35 V at different temperatures, is illustrated in Figs. 6 and 7, respectively. It can be seen, for example in Fig. 6, that we could not get experimental lifetime for devices pulsed stressed with – 35 V at 150 °C since in this case ΔV_T did not reach 50 mV even after 72 hours of stressing. Thus, duration of the experiment in this case was not sufficient to achieve ΔV_T as high as FC, which means the stress time should have been extended to exceed the device lifetime for a given combination of stress bias and temperature. However, this could require the stressing to be done beyond the reasonable time limit, so in such cases it is convenient to use an adequate fitting model capable to provide reliable prediction of ΔV_T on the bases of available data. There are several well-established fitting models for prediction of ΔV_T, such as regular exponential model, 2-tau exponential model and stretched exponential model [27-30]. The best fit to our experimental results on power VDMOS devices was found to yield the stretched exponential model, which is given by [12, 29, 30]:

$$\Delta V_T(t) = \Delta V_{T\max} \cdot [1 - \exp(-(t/\tau_o)^{\beta})] \quad (1)$$

where ΔV_{Tmax}, τ_o, and β are the fitting parameters. Both experimental and fitting results for threshold voltage shifts during the pulsed NBT stressing of IRF9520 p-channel power devices with – 35 V at 150 °C are shown in Fig. 6. As can be seen, experimental lifetime $\tau 6$ is obtained as the time required that stretched exponential fit for ΔV_T reaches 50 mV. Similarly, stretched exponential fits were used in Fig. 7 to obtain the experimental lifetime values $\theta 5$ and $\theta 6$ for devices pulsed stressed with – 35 V at 150 °C and 125 °C.

3.2. Extrapolation to normal operating voltage

Extrapolation along the voltage or electric field axis by any of the commonly used models, such as V_G, $1/V_G$ and power-law models, which are based on corresponding degradation models for the threshold voltage shifts

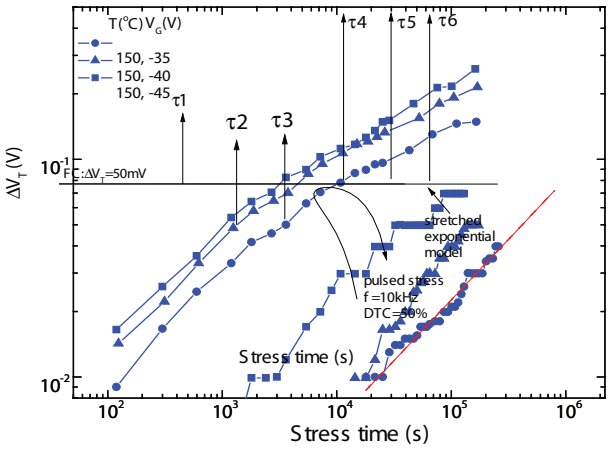

Figure 6: Extraction of experimental lifetime from the threshold voltage shift time dependencies recorded during the NBT stressing with different gate voltage magnitudes at $T = 150$ °C.

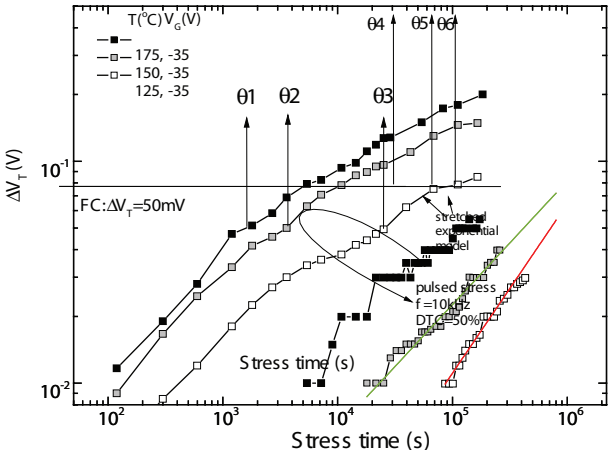

Figure 7: Extraction of experimental lifetime from the threshold voltage shift time dependencies recorded during the NBT stressing with gate voltage $V_G = -35$ V at different temperatures.

[9, 10], requires experimental lifetime values extracted from the data obtained by stressing with different voltages at constant temperature, such as those shown in Fig. 6. Here we use the $1/V_G$ model to estimate lifetime in devices subjected to NBT stress, which is illustrated in Fig. 8 a) for static and b) for pulsed bias conditions. Only extrapolation to $V_G = -20$ V is shown, but the procedure can be used to estimate the lifetime by extrapolation to any other reasonable operation voltage. The procedure additionally allows for estimation of another reliability parameter, so-called "ten year operation voltage", V_{G10Y}, which is defined as maximum gate voltage that allows 10 years of device operation at given temperature so that stress-induced threshold voltage shift remains below the FC. In Fig. 8 only the V_{G10Y} value for devices stressed at 125 °C is indicated, but the values for the other two stress temperatures can be read as well. As can be seen, there are significant differences in lifetime and ten year operation voltage values between devices stressed under the static and pulsed NBT stress conditions. The lifetime values obtained by extrapolation to – 20 V are more than two orders of magnitude higher under the pulsed gate bias conditions (XP1, XP2, XP3) than under the static ones (XS1, XS2, XS3). Also, the ten year operation voltage is 5÷8 V higher under the pulsed voltage regime ($V_{G\ 10Y}^{P}$) than under the static one ($V_{G\ 10Y}^{S}$). These findings indicate that in many real applications of p-channel power MOSFETs, where gate bias switches between the "high" and "low" levels, devices may maintain their proper functionality much longer than if kept constantly under the dc bias.

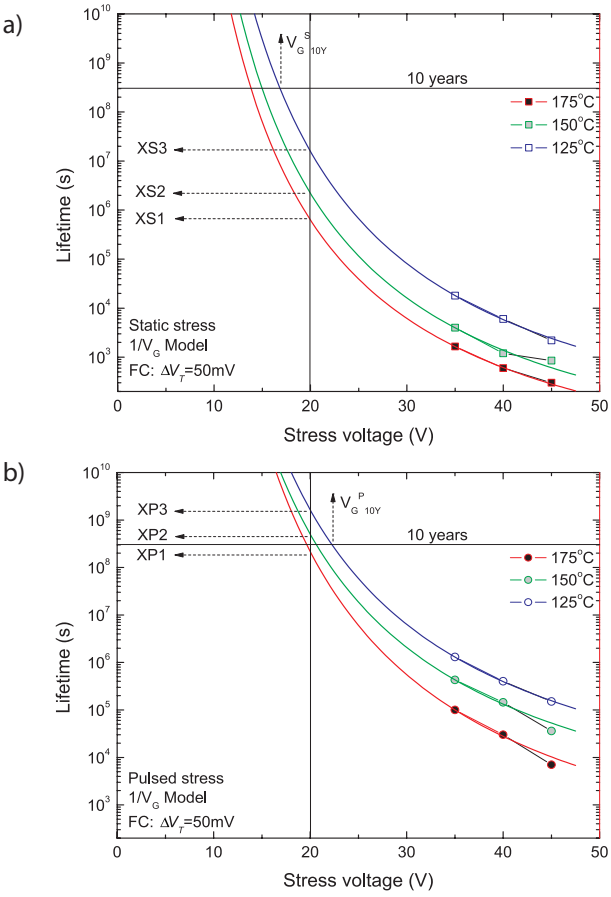

Figure 8: Extrapolation to normal operation gate bias by means of $1/V_G$ model to estimate the lifetime and ten year operation voltage in p-channel power VDMOSFETs subjected to a) static and b) pulsed NBT stressing.

3.3 Extrapolation to normal operating temperature

The $1/V_G$ and other models for extrapolation along the voltage or electric field axis can be used to estimate device reliability parameters (lifetime and ten year operation voltage) for any operating voltage, but only at temperatures applied during accelerated stress experiments, which are generally higher than actual temperatures found in device normal operation mode.

Estimates obtained by these models are very convenient as the worst case expectations, but it could be very useful if possible to estimate the lifetime for normal operation temperatures as well. As a possible solution, we have recently proposed the use of suitable model for extrapolation along the temperature axis [11-13]. The model is easily derived from any of several degradation models for NBT stress-induced threshold voltage shift, which all include the Arrhenius temperature acceleration factor, and can be expressed as:

$$\tau = A \cdot \exp(B / T), \quad (2)$$

where A and B are the fitting parameters taken from the initial degradation model. This model apparently takes the same mathematical form as $1/V_G$ model, and is thus called "1/T" model.

The use of 1/T model requires experimental lifetime values extracted from the data for NBT stressing performed with the same voltage magnitude at several different temperatures, such as those plotted in Fig. 7. The lifetime estimation by means of this model is illustrated in Fig. 9. Only extrapolation to T = 100 °C (which seems rather realistic for operation of power devices) is shown, but the same procedure can be used to estimate device lifetime by extrapolation to any other reasonable operation temperature. Fig. 9 also illustrates that extrapolation procedure by means of the 1/T model, in analogy with the $1/V_G$ model, allows for estimation of an additional reliability parameter, which is accordingly called "ten year operation temperature", T_{10Y}, and is defined as maximum temperature that allows 10 years of device operation under given V_G so that stress-induced ΔV_T remains below FC. As can be seen, 1/T model also yields significant differences between the effects of static and pulsed NBT stress. The lifetime at 100 °C is about two orders of magnitude higher under the pulsed bias conditions (YP1, YP2 and YP3) than under the static ones (YS1, YS2 and YS3). Also, the ten year operation temperature is 8÷18 °C higher under the pulsed regime (T^P_{10Y}) than under the static one (T^S_{10Y}). These observations are completely in line with those obtained by means of $1/V_G$ model.

3.4 Double extrapolation along the voltage and temperature axes

Each of the two extrapolation procedures considered so far disregards one of the stress acceleration factors, either temperature or voltage, so both procedures may underestimate device reliability parameters. The goal of our study was to estimate the lifetime of investigated VDMOSFETs under normal operating conditions (both voltage and temperature) using the results obtained by accelerated NBT stressing. A reasonable solution could be found by combining the two procedures, i.e. by performing two successive extrapolations along the gate voltage (or corresponding electric field) and temperature axes, where the latter extrapolation uses the results of the former one as the input data [11, 12]. This is shown in Fig. 10, which illustrates extrapolation along the temperature axis to 100°C by 1/T model, where the results of previous extrapolation along the voltage axis to – 20 V by $1/V_G$ model from Fig. 8 (XS1, XS2, and XS3 for static stress; XP1, XP2, and XP3 for pulsed stress) have been taken as the input data. As can be seen, the two successive extrapolations yield a single lifetime projection to (– 20 V, 100 °C) for each of the two operating regimes considered (τ_{0S}, for static, and τ_{0P}, for pulsed regime). The order of performing the two extrapolations can be reversed: the YS1, YS2, and YS3 data (for static stress) and YP1, YP2 and YP3 data (for pulsed stress) from Fig. 9, obtained by extrapolation to a normal operation temperature by the 1/T model can be further used for extrapolation to a normal operation voltage by $1/V_G$ model, which is illustrated in Fig. 11. The two τ_{0S} values obtained in Figs. 10 and 11

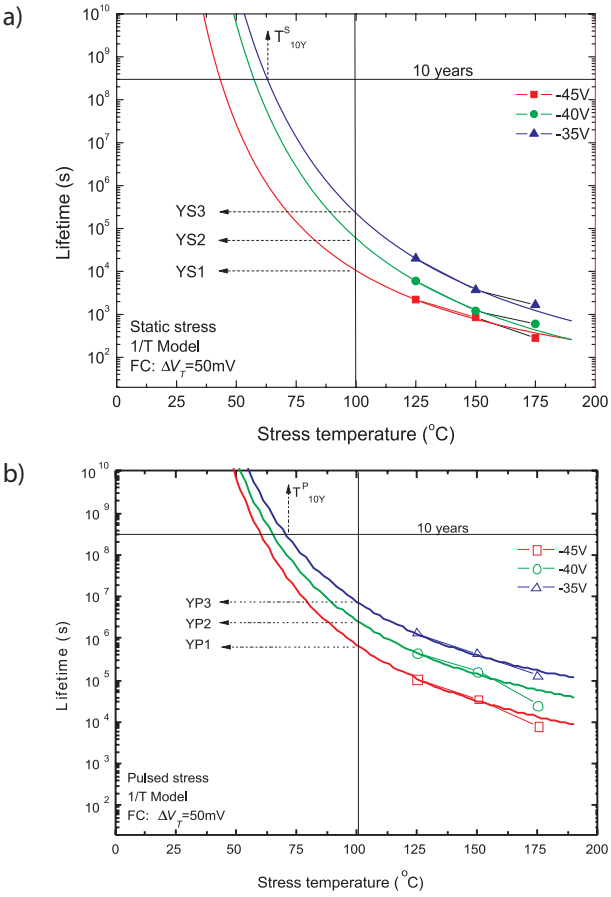

Figure 9: Extrapolation to normal operation temperature by means of 1/T model to estimate the lifetime and ten year operation temperature in p-channel power VDMOSFETs subjected to a) static and b) pulsed NBT stressing.

are close one to the other, and the two τ_{0P} values also are, so the order in performing the two extrapolations does not seem to be of great importance. Also, the results in both figures suggest the device lifetime under the pulsed operation regime could be more than one order of magnitude longer than under the static one. Yet, there are certain differences between the two τ_{0S} values, as well as between the two τ_{0P} values, obtained by the two procedures shown in Figs. 10 and 11. These differences, which are measure for the uncertainties in estimated lifetime values, could be associated with and may depend on variations in stress conditions applied, level of stress-induced degradation taken as the failure criteria, and features of the models used for extrapolation to normal operation conditions [12]. These uncertainties might be lesser if both extrapolation procedures were applied in parallel, so the average of the two estimated lifetime values could be taken as the most probable true lifetime.

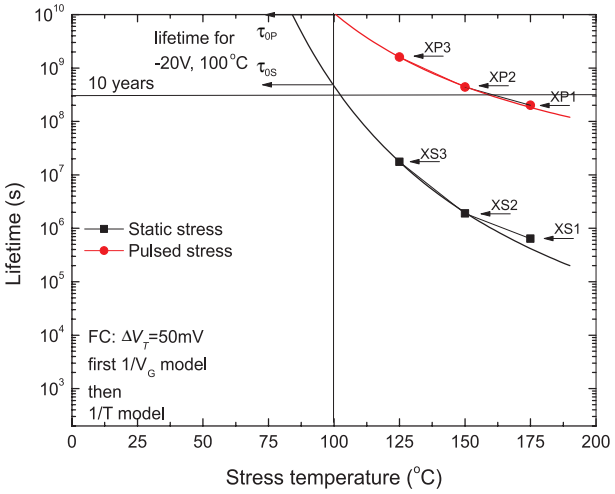

Figure 10: Lifetime extrapolation to normal operating conditions by 1/T model with input data taken from Fig. 8.

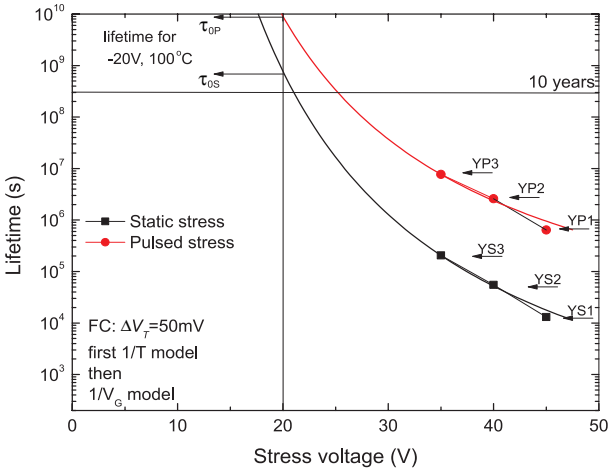

Figure 11: Lifetime extrapolation to normal operating conditions by $1/V_G$ model with input data taken from Fig. 9.

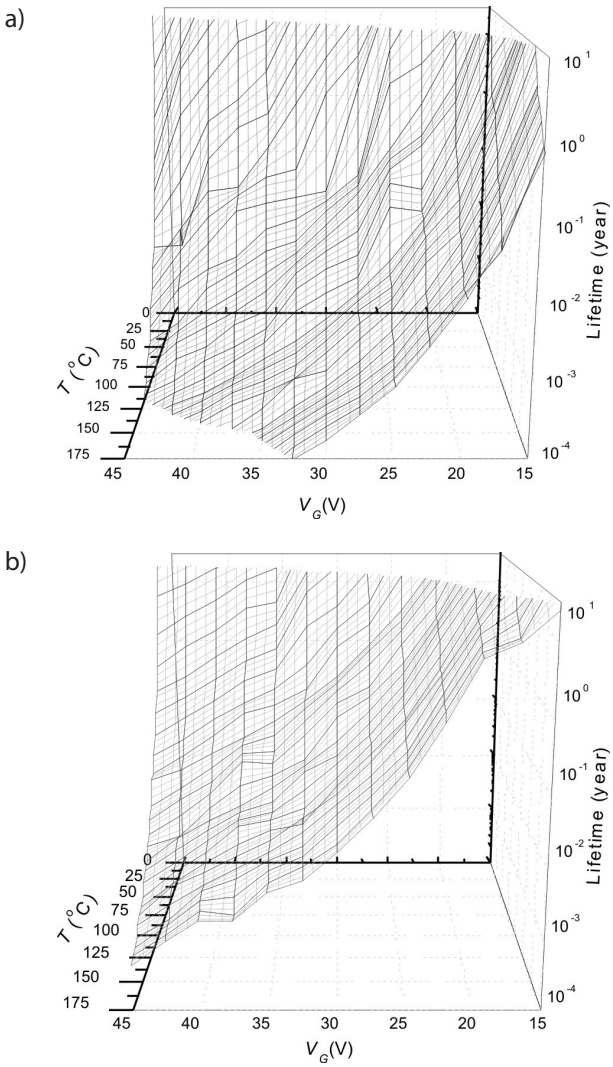

Figure 12: Surface areas representing the lifetime estimates in: a) static and b) pulsed NBT stressed devices for a full range of operating voltages and temperatures with ΔV_T =50 mV taken as a failure criterion.

The 1/T model for extrapolation along the temperature axis may be combined for double extrapolation not only with $1/V_G$ model but also with other models for extrapolation along the voltage axis (V_G model, power law model), where the best choice should be the model that provides the best fit to the data. It is also important to note that double extrapolation approach can be used to estimate device lifetime for any reasonable combination of operating voltages and temperatures, which means the procedure can be re-done for each combination falling within the entire range of operating voltages and temperatures. The set of results obtained in this way can be used to construct the surface area representing the lifetime values corresponding to a full range of device operating conditions. The approach has been applied to our experimental results for static and pulsed NBT stressed p-channel power VD-

MOS devices IRF9520, and Fig. 12 shows such surface areas representing lifetime projections to a full range of operating temperatures and gate voltages for devices operated under the a) static and b) pulsed stress conditions (threshold voltage shift of 50 mV has been taken as the failure criterion in both cases). As can be seen, surface area constructed for the static NBT stress appears to fall below the one for the pulsed stress, which means the lifetime is longer under the pulsed stress conditions than under the static ones independently on the choice of operation voltage magnitude and/or temperature. The appropriate surface areas can be created for different failure criteria, and may help in estimating either the lifetime or maximum allowed voltage and temperature for every single device in the operation environment.

4. Conclusion

NBT stress-induced threshold voltage shifts in p-channel power VDMOSFETs under the static and pulsed stress conditions were compared in terms of the effects on device lifetime. The $1/V_G$ model, for extrapolation along the voltage axis, and 1/T model, for extrapolation along the temperature axis, were used to get lifetime estimates for the voltages and temperatures expected in device normal operation mode. As a consequence of the shorter actual stress time and dynamic recovery effects, threshold voltage shifts were less significant under the pulsed stress conditions. Accordingly, estimated lifetime was much longer under the pulsed stress conditions than under the static ones, as shown by using each of the above two models individually, as well as by combined use of both models for double extrapolation along both voltage and temperature axes. Finally, double extrapolation approach was shown to allow for construction of the surface area representing lifetime values corresponding to a full range of device operating voltages and temperatures.

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