

Orthodox Theory Monte-Carlo Simulation of Single-Electron Logic Circuits

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Abstract: In the past decades MOS based digital integrated logic circuits have undergone a successful process of miniaturisation eventually leading to dimensions of a few nanometres. With the dimensions in the range of a few atomic radii the end of conventional MOS technology is approaching. Amongst the prospective candidates for sub 10nm logic are integrated logic circuits based on single-electron devices. In our contribution we present the use of MOSES (Monte-Carlo Single-Electronics Simulator) as a method for simulation of complementary single-electron logic circuits based on the orthodox theory. Simulations of single-electron devices including a single-electron box, a single-electron transistor and a complementary single-electron inverter were carried out. Their characteristics were evaluated at different temperatures and compared to measurement results obtained at other institutions. The potential for room-temperature operation was also assessed.

Keywords: single-electron logic circuits; single-electron transistor; Monte-Carlo; simulation; MOSES; voltage-state logic

Monte-Carlo simulacija enoelektronskih logičnih vezij na podlagi Ortodoksne teorije

Izveček: V preteklih desetletjih je MOS tehnologija uspešno prestala proces miniaturizacije, kar je privedlo do dimenzij struktur v rangu nanometrov. Dimenzije, ki obsegajo le še nekaj atomski polmerov, bi lahko napovedovale konec konvencionalne MOS tehnologije. Kot eden izmed glavnih kandidatov za logična vezja, ki bodo delovala pri dimenzijah okoli 10nm in manj, se omenjajo logična vezja na osnovi enoelektronskih gradnikov. V našem prispevku bomo predstavili uporabo simulacijskega orodja MOSES (Monte-Carlo Single-Electronics Simulator), kot metode za simulacijo komplementarnih enoelektronskih digitalnih logičnih vezij na podlagi Ortodoksne teorije. Izvedli smo simulacije enoelektronskih struktur vključno z enoelektronsko škatlo, enoelektronskim tranzistorjem in komplementarnim enoelektronskim inverterjem. Njihove karakteristike smo ovrednotili pri različnih temperaturah in primerjali z izmerjenimi karakteristikami z drugih raziskovalnih ustanov. Ocenili smo tudi možnost delovanja enoelektronskih vezij pri sobni temperaturi.

Ključne besede: enoelektronska logična vezja; enoelektronski tranzistor; Monte-Carlo; simulacija; MOSES; logika stanj napetosti

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1 Introduction

In the last 50 years since the invention of CMOS technology in 1963 the aforementioned technology has gained a huge advantage mainly due to its small power dissipation. Through the continuous process of miniaturisation the reduction of device dimensions from 5 μm to 14 nm was achieved [1]. Conventional CMOS technology is bound to reach its limits in the near future and in order to sustain device miniaturisation other technological options should be employed.

One of the prospective candidates for the implementation of sub-10 nm digital logic circuits are digital logic

circuits based on single-electron Coulomb blockade devices [2]. The possibility to manipulate electrons one by one should reduce the power dissipation and enable higher integration densities. Up to this point two implementation abilities have been explored. Voltage-state logic as a direct transfer of CMOS topology to single-electron devices [3] and charge-state logic in the form of binary decision diagram – BDD [4] circuits and quantum cellular automaton – QCA [5][6] circuits.

In our contribution we explore the possibility of voltage state logic circuits design and analysis using the MOSES [2] Monte-Carlo simulator. Our focus will be mainly on

the implementation of logic functions with means of complementary single-electron logic circuits based on the Orthodox theory briefly described in Section 2.

2 Orthodox theory and monte-carlo simulation

In order for single-electron charging effects to become observable and for orthodox theory to apply two conditions should be met. Firstly charging energy should be much greater than thermal energy as depicted in equation (1).

$$E_C \gg E_T \tag{1}$$

This condition requires either feature sizes to be in the range of nanometres to minimise capacitances of the structure, or the operating temperature to be near the absolute zero. The second condition to be met is the condition of tunnel resistance R_t in equation (2).

$$R_t = \frac{\hbar}{q^2} \approx 4.2 \text{ k}\Omega \tag{2}$$

Satisfying these conditions, one can analyse single-electron circuits according to the orthodox theory. Applying the theory, the tunnel rate Γ through an individual junction can be expressed by means of equation (3).

$$\Gamma = \frac{\Delta E}{q^2 R_t \left(1 - \exp\left(-\frac{\Delta E}{k_B T}\right) \right)} \tag{3}$$

As the orthodox theory assumes independence between individual tunnelling events and only one tunnelling event possible at a certain time, it is possible to describe the macroscopic behaviour of such circuit through a stochastic series of such tunnelling events. The process takes into account probabilities that a tunnelling event will occur at a certain point in time and the probabilities are weighted by the tunnelling rate Γ . Such a process is suitable for implementation within the Monte-Carlo method and is implemented in the MOSES simulator.

3 Simulation of single-electron structures

Within our work we have analysed circuits of a single-electron box, single-electron transistor and a comple-

mentary single-electron inverter. Wherever possible we compared our results to measurements of a physical device with similar parameters taken at other institutions.

3.1 Single-electron box

A single-electron box is the simplest single-electron structure. It consists of a single tunnel junction, coupled through a capacitance to a voltage source. The circuit is shown in Fig. 1 and circuit parameters used for simulation are given in the Table 1 below.

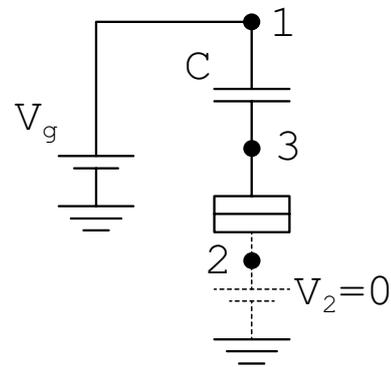


Figure 1: Circuit of a single-electron box used for simulation.

Table 1: Single-electron box circuit parameters used for simulation.

Element	Value
C	9 aF
C_{TJ}	1 aF
R_{TJ}	100 k Ω
V_g	0-50 mV

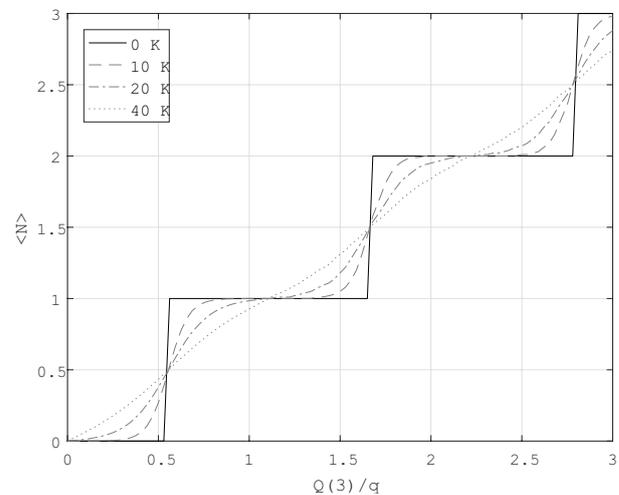


Figure 2: Simulation results of a single-electron box at 25 mK.

Varying the voltage V_g from 0 to 50 mV, we observed a characteristic response of the circuit – Coulomb staircase, predicted by the orthodox theory. Simulation results are shown in Fig. 2.

We could not find a real structure measurement to compare the results to, but we have found them comparable to an identical structure simulated by MUSES [7], which is another Monte-Carlo simulator.

The characteristic Coulomb staircase is temperature dependent, since the thermal energy should not exceed the charging energy. Simulation of the temperature dependence of a Coulomb staircase is depicted in Fig.3.

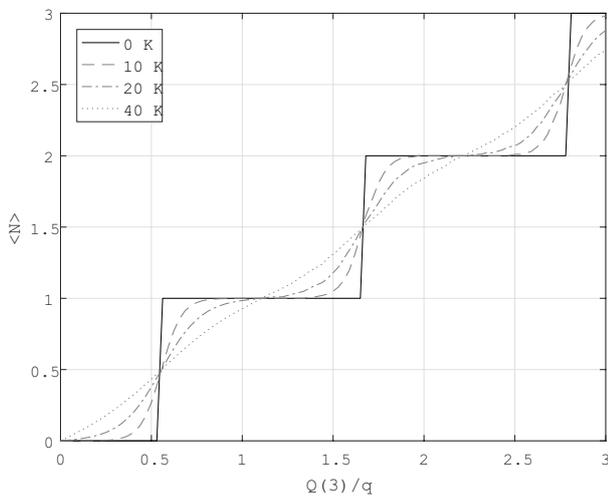


Figure 3: Temperature dependence of the Coulomb staircase.

3.2 Single-electron transistor

A single-electron transistor (SET) is a modification of a single-electron box. Adding another tunnel junction and a supply voltage source, we get the circuit presented in Fig. 4. In Table 2 element values used for simulation are presented.

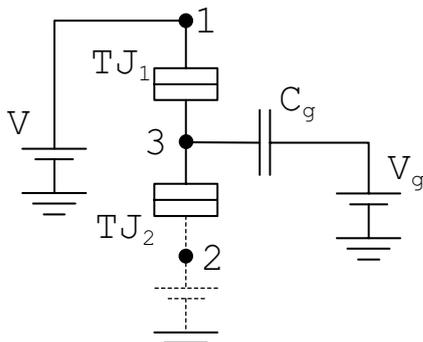


Figure 4: Circuit of a single-electron transistor used for simulation.

Values for the simulation were chosen according to the measurements in [8]. Varying the gate voltage V_g and supply voltage V as given in Table 2, we were able to obtain a stability diagram for the given transistor. The simulation was performed at 25 mK and a background charge at the central island of 0.3 electrons as observed in [8]. The addition of background charge was necessary to achieve agreement between simulations and measurements, since it shifts the stability diagram of a single-electron transistor. The obtained stability diagram is given in Fig. 5. Fig. 6 presents a measured stability diagram of a real single-electron transistor [8] with the same parameters.

Table 2: Single-electron transistor circuit parameters used for simulation.

Element	Value
C_{TJ1}	57.14 aF
C_{TJ2}	53.94 aF
C_g	3.2 aF
R_{TJ1}, R_{TJ2}	100 kΩ
V_g	0-80 mV
V	0-2 mV

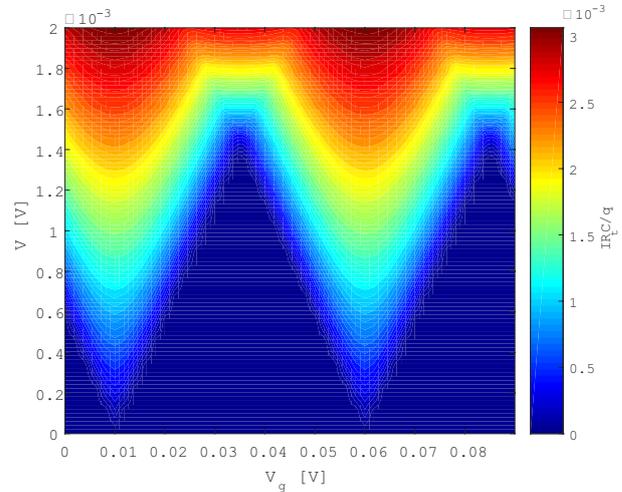


Figure 5: Simulation of a SET stability diagram at 25 mK.

3.2.1 Temperature dependence

As a single-electron transistor is just a variation of a single-electron box, its characteristics should also be temperature dependent. Taking 114.28 aF as a cumulative capacitance of the circuit in Fig. 4 towards the environment C_Σ , we were able to estimate the temperature, up to which Coulomb oscillations would be noticeable, according to equation (4).

$$T \ll \frac{q^2}{k_B C_\Sigma} \approx 16 K \tag{4}$$

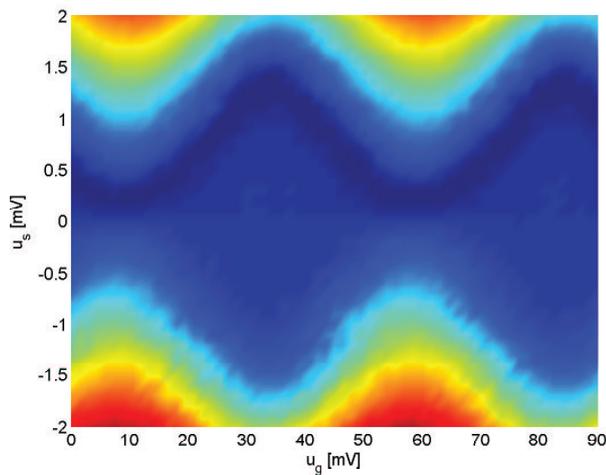


Figure 6: Measurement of a SET stability diagram at 25 mK [8].

To get a sense of the relation ‘far less’ in equation (4), we made a simulation of Coulomb oscillations at different temperatures and a supply voltage V of 1 mV. It was observed, that Coulomb oscillations become negligible at temperatures 3 times smaller as calculated. The results of the simulations are given in Fig. 7.

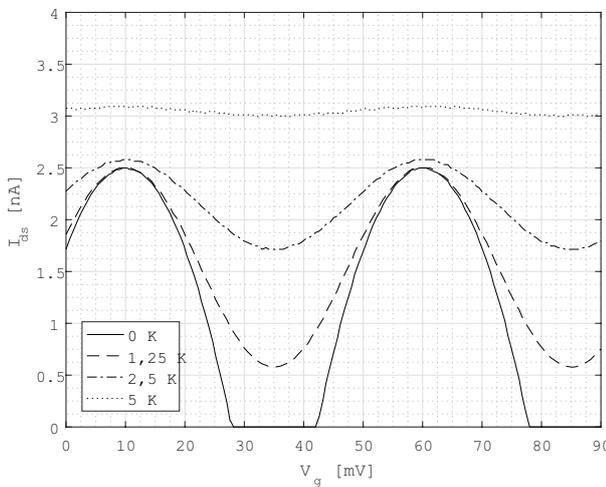


Figure 7: Simulation of Coulomb oscillations at different temperatures. $V = 1$ mV.

As the temperature dependence of the observed Coulomb oscillations may not pose a serious problem at this point, their impact of the characteristics of complementary single-electron logic circuits is quite significant.

3.3 Complementary single-electron inverter

A complementary single-electron inverter is comprised of two single-electron transistors much as a

conventional CMOS inverter. The two identical SETs with an additional controlling capacitance at the gate, act as a p-MOS or n-MOS equivalent, depending on the operating point set by the controlling electrodes. The schematic of a single-electron inverter circuit is shown in Fig. 8. The elements’ values were once again taken from a real implementation of the device from [8] for easier comparison of the results. The parameters are given in Table 3.

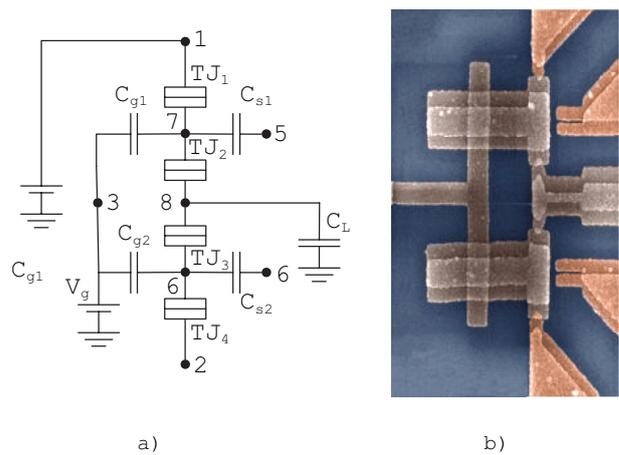


Figure 8: Complementary single-electron inverter a) and an electron microscope image of the realisation from [9] b).

Table 3: Single-electron inverter circuit parameters used for simulation.

Element	Value
$C_{TJ1} - C_{TJ4}$	100 aF
C_{g1}, C_{g2}	800 aF
C_{s1}, C_{s2}	686 aF
$R_{TJ1} - R_{TJ4}$	100 kΩ
V_g	0-80 μV
V_s	65 μV

The simulation was performed at 25 mK and with no background charge at any of the nodes, since none was reported originally. Fig. 9 shows simulation results of a DC transfer characteristics compared to the measurement and SPICE simulation results obtained in [8].

Our simulated characteristic shows some deviations from the measured one and more closely corresponds to the characteristics obtained by SPICE. The difference is thought to be due to second-order effects namely cotunneling, since it is not simulated by MOSES and could result in a steeper characteristic than in reality. Second-order effects are most prominent near or in the Coulomb blockade region [10], where standard tunneling is negligible. Additional electron transmission

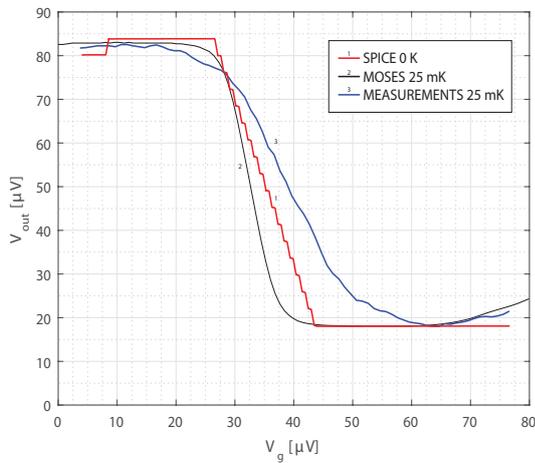


Figure 9: Simulated SET inverter characteristics at 25 mK from MOSES, SPICE [8] and the measurement of the device [8].

through the single-electron transistor induced by the cotunneling effect in the Coulomb blockade region could account for the gentler slope, since it inhibits charging and discharging of the load capacitor. Nearly perfect agreement between simulations and measurements outside of the transition region of the inverter, on the other hand, lets us believe that simulations at higher temperatures should show similar or even better agreement with real structures, due to the diminishing of the cotunneling effect with increasing temperature as observed in [11-12].

3.3.1 Temperature dependence of DC transfer characteristic

The temperature dependence of the inverter’s transfer characteristic was evaluated using equation (4) where the cumulative capacitance towards its surroundings 1686 aF was taken as the value of C_{Σ} . Taking into account the factor ‘far less’ derived in the previous section,

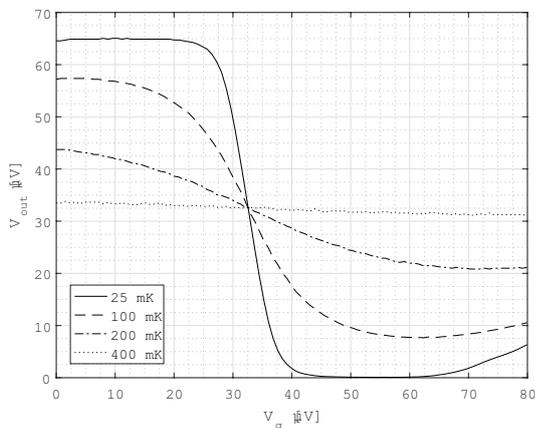


Figure 10: Temperature dependence of SET inverter characteristics.

the maximum operating temperature was estimated to be around 360 mK. The simulation of the temperature dependence of the inverter’s DC transfer characteristic is shown in Fig. 10.

From Fig. 10 one can clearly see a continuous degradation of logic levels with increasing temperature, as well as a decrease in the absolute differential gain at the switching point. An inverter with such characteristics is clearly an inappropriate building block for larger logic circuits even at temperatures close to absolute zero, let alone at room temperature.

3.3.2 Single-electron inverter at room temperature

The main goal in developing single-electron circuits is room temperature operation. According to the simulations from previous sections we have proposed a structure that when implemented, should exhibit single-electron effects even at room temperature. Using equation (4) and a factor 1/5 for the criterion ‘far less’ we have estimated the value of C_{Σ} to less than 1.2 aF.

To meet the criterion we have scaled the values in Table 3 2000 times. The element values of the scaled inverter are given in Table 4 and the simulation of the DC transfer characteristics at different temperatures is given in Fig. 11.

Table 4: Single-electron inverter circuit parameters used for simulation.

Element	Value
$C_{TJ1} - C_{TJ4}$	0.05 aF
C_{g1}, C_{g2}	0.4 aF
C_{s1}, C_{s2}	0.343 aF

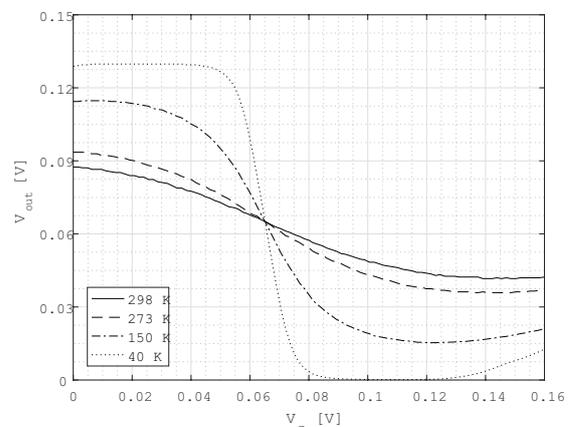


Figure 11: Temperature dependence of SET inverter characteristics.

From Fig. 11 it is clearly visible, that the inverter characteristic is still observable at room temperature, even

though the differential gain at the switching point is already below 1. A strong degradation of logic levels is also visible. Despite the observable inverter characteristics at room temperature, the inverter would still not be capable to drive further logic stages. For that to become possible, the dimensions of the features composing the inverter would need to drop into the sub-nanometre region as predicted in [13].

The dimensions of a fabricated device with parameters from Table 4, where each island is shaped as a cube for simplicity, are given in Table 5. Fig. 12 presents a simplified layout of the device.

Table 5: Dimensions of the single-electron inverter structure for parameters in Table 4 and Table 3.

Dimension	Length Table 4	Length Table 3
a	1 nm	1 nm
b	2.38 nm	106 nm
c	0.12 nm	0.12 nm
d	0.15 nm	0.15 nm

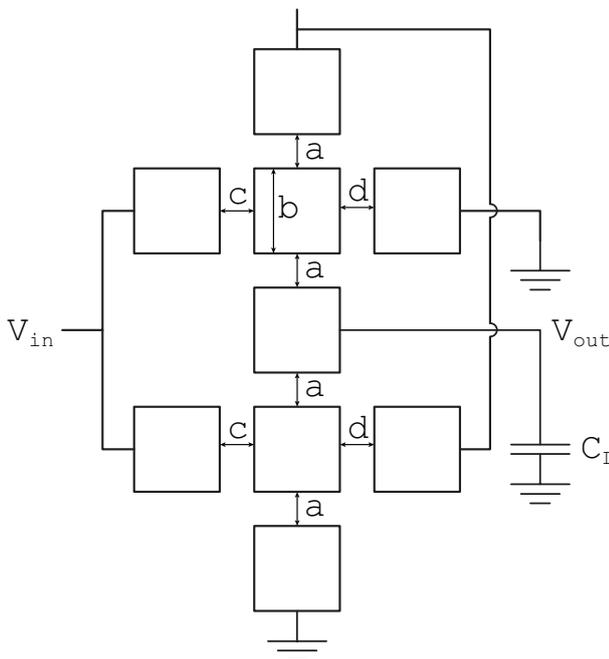


Figure 12: Proposed simple layout of a room temperature operable single-electron inverter.

4 Conclusions

From the performed simulations it is clear, that single-electron circuits could be the next step in the integration and miniaturisation of logic circuits. One of the setbacks of complementary single-electron logic is the

small dimension of the features comprising the single-electron circuits to achieve room temperature operation. Another possible setback is the degradation of the logic levels and thus the inability to drive further stages. The solution of the problem could be found in single-electron charge state logic, which defines logic levels with the presence of an electron and not with the voltage level as do complementary single-electron circuits. Two of the possible approaches already in development are the use of QCA (Quantum Cellular Automaton) [5][6] and the BDD (Binary Decision Diagram) [4].

5 References

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