# On-line Testing and Recovery of Systems with Dynamic Partial Reconfiguration

Anton Biasizzo

Inštitut Jožef Stefan

Jamova 39, 1000 Ljubljana, Slovenia

E-Mail: anton.biasizzo@ijs.si

The FPGA devices are increasingly being used in mission critical systems like security systems, banking systems, avionics, etc. The radiation induced errors that corrupt the configuration memory of the FPGA device are a major concern for the system reliability and dependability. These errors are very frequent in the space environment; however, due to the increasing integration density they become significant also at the earth surface.

Different fault-tolerant techniques are developed to increase the reliability and dependability of the system. On-line testing detects the errors in the system, while the system performs its task. Error mitigation techniques enable the system to operate correctly even in the presence of few errors. Error recovery techniques recover the system to its original state after a fault occurred.

The error recovery techniques of the FPGA device restore the configuration memory. This can be done by periodically reconfiguring the whole device or by more advanced dynamic partial reconfiguration, where the error is detected and the affected part of the configuration memory is restored. Dynamic partial reconfiguration method employs error-recovery mechanism, which is independent of the application. It uses the FPGA configuration interface to detect the errors within the configuration memory and to restore faulty configuration parts to their original state. Error recovery mechanism could be implemented as an external device or internally, using some of the FPGA resources. The internal error recovery mechanism is also susceptible to FPGA configuration error thus an additional error mitigation technique should be used in the case of very reliable system. The triple module redundancy implementation of the internal error recovery mechanism drastically increases the system reliability while it occupies a small amount of FPGA resources.