# Design Aspects for Ultra-low Voltage Circuits

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Implantable biomedical applications have very stringent constraints on energy dissipation, as replacing batteries are of discomfort for the patient, and sometimes not even possible, e.g., the cardiac pacemaker. In order to meet energy constraints system-on-chip solutions are realized, and with shrinking technologies leakage power is identified as one of the major design concerns.

Aggressive supply voltage scaling down to near- or sub-threshold (sub-VT) levels is a very efficient technique to increase the energy efficiency of digital circuits. The penalties due to performance degradation and reliability are severe, and need to be addressed. Traditional design space exploration techniques need to be revised, and new modeling approaches are required. In this paper the efficiency of pipelining, balancing, and time-multiplexing is discussed by applying a (sub-VT) model for energy profiling. A seamless integration of full-custom gates, which are optimized for sub-VT operation, is discussed by use cases. A competitive approach to static random access memory (SRAM) hard macros based on standard-cell memories (SCMs) is proposed and validated with measurements in 65-nm CMOS technology.