**Društvo MIDEM**

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Vas vljudno vabi na predavanje

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 “**Material and Device Challenges for Future CMOS Technologies**”.

Predavanje bo

v sredo, 4.4.2018 ob 14:00 uri v predavalnici P1

na Fakulteti za elektrotehniko, Tržaška cesta 25, Ljubljana.

Predavanje bo potekalo v angleščini.

**Abstract:**

CMOS devices, driven by minimum device geometry, performance enhancement, cost issues and low power consumption, are achieved by using optimizing process modules, introducing new materials and implementing novel device concepts. Stress engineering, ultra-shallow junctions, high- gate-stacks, optimized process sequences (e.g. gate-first vs replacement gate or gate-last), raised source/drain, use of high-mobility materials etc. are studied. Improved drive currents and electrostatic control trigger the exploration of Multi-gate devices (MuGFETs). FD SOI technologies with ultra-thin body and buried oxide (UTBB SOI) have potential down to the 10 nm mode. Tunnel-FETs (TFETs), relying on band-to-band-tunnelling and allowing steep subthreshold swings are gaining interest. Further scaling leads to gate-all-around and nanowire devices. Optimized epitaxial growth resulted in the fabrication of Ge (p-channel), III-V (n-channel) or hybrid Ge/III-V devices on a Si substrate. High mobility materials are implemented in TFET and nanowire structures. Challenges of some key process modules and device structures are discussed. Hot topics like 2D materials and devices and spintronic computing are addressed.