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on Microelectronics,
Devices and Materials*

The Workshop on Integrated Photonics



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FOREWORD

Dear colleagues,

Welcome to the 61st International Conference on Microelectronics, Devices and Materials, (MIDEM 2026) with the joint Workshop on Integrated Photonics. The conference continues the tradition of annual, international meetings organized by MIDEM – Society for Microelectronics, Devices and Materials. These conferences have consistently attracted a large number of Slovene and foreign experts, as well as distinguished invited speakers, providing an opportunity for them to present their activities and research progress to the international audience and discuss trends and problems related to their fields of work.

This year, 50 regular contributions and 7 invited lectures will be presented over the three days, from September 28th to September 30th, 2026. Conference contributions are grouped into the following sections: Materials, Technology and Devices; Thin and Thick Films; Sensors and MEMS; Integrated Circuits and Electronics; Optoelectronics; and the Students Section. On the second day of the conference, the Workshop on Integrated Photonics is organised.

We would like to express our gratitude to the invited speakers and contributors of regular papers for their valuable scientific contributions to the conference sessions and the workshop. The members of the International Scientific Board are gratefully acknowledged for their active support of the conference. We also thank all the Session Chairs and the members of the Conference Organising Committee, who did their best to make the conference a success.

We hope that you will remember this event, not only for the importance of the papers and discussions, but also for the new friendships and the pleasant memories of the country.

We wish you a pleasant stay in Ljubljana and in Slovenia.

Matija Pirc, conference chairperson and
Andraž Debevc, workshop chairperson

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**CONFERENCE
INVITED PAPER**

Flexible composites for energy storage and harvesting: how material design and processing affect functional properties

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Flexible ferro/piezoelectric polymer composites are promising materials for wearable and deformable electronics, where mechanical flexibility must be combined with high functional performance. In particular, composites based on PVDF (poly(vinylidene fluoride)) and ferroelectric perovskite fillers combine the flexibility, chemical stability and high breakdown strength of polymers with the enhanced dielectric and electromechanical response of ceramic inclusions. These materials are investigated for energy harvesting and storage, as well as sensing and actuation applications.

The functional response of PVDF-based composites is strongly governed by processing, the quality of the interface between the dissimilar materials, and the overall microstructure. Filler size, morphology, dispersion, and volume fraction affect the dielectric and piezoelectric properties of the composite, while also promoting the formation of the polar β -phase of PVDF, the polymorph with the highest dipole moment. The various processing routes, including advanced manufacturing techniques, critically influence filler distribution, phase content, and interfacial interactions, ultimately controlling macroscopic electrical behavior.

This contribution will review the effect of processing on the materials properties relevant to applications and recent advances in the microstructure engineering of ferro/piezoelectric polymer matrix composites, with emphasis on interface design between polymer matrices and inorganic nanoparticles. Surface modification strategies, including oxide-shell coatings, are discussed as effective approaches to tailor local electric field distribution and optimize composite performance.

**WORKSHOP ON
INTEGRATED PHOTONICS
PLENARY LECTURE**

Silicon photonics: emerging trends, opportunities and challenges

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Silicon photonics is rapidly transitioning from a relatively homogeneous and monolithic technology used primarily for data center interconnect to a diverse and heterogeneous technology family serving a much broader array of applications. While this opens the door to further scaling of the impact of photonic integration on various markets, it also comes with new challenges. Building viable industrial supply chains that can handle the material and technology diversity is one of those challenges.

**WORKSHOP ON
INTEGRATED PHOTONICS
INVITED PAPERS**

Photonic Integrated Circuits for Signal Processing and Computing

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After a brief panorama of the potentials and limits of the integrated photonic platform to implement passive and active functionalities, and the electronic and software control layer required for fully exploit and scaling the technology, the main concepts of analog photonic processing are introduced. The two key operations, multiplication and sum, are explored and combined to realize matrix and simple algebra functions up to programmable processors.

Analog processing of information performed directly in the optical domain has enormous potential for processing large bandwidth signals yet preserving information on amplitude, phase and polarization, manage advanced modulation formats, WDM signals and even chaotic light and quantum states. In this contribution we present the principle of operation of an integrated photonic processors based on meshes of Mach-Zehnder interferometers with a control layer that can be monolithically integrated in the photonic chip and its application for mitigating the typical atmospheric effects in a Free Space Optical communication link with classical and chaotic light, compensated the effects of multimode/multicore fiber transmission link and the exploitation as beam analyzer to perform optical wavefront mapping and spatial coherence estimation.

In particular, an integrated photonics processor-based transceiver capable of compensating for scintillation and wander induced by atmospheric turbulence automatically, without any need of knowledge of the media itself is presented. Bidirectional 25Gbit/s OOK signals are successfully transmitted on an indoor setup emulating 1km long link.

Further, we demonstrated the transmission over a multi-core fiber enabled by all-optical multiple-input multiple-output (MIMO) demultiplexing. We demultiplex optically all 10 Gbaud PDM-QPSK channels transmitted over 5 km of randomly-coupled 4-core fiber.

Control, scalability and system consideration are discussed, as well as sensing applications, such as measure the phase front of the incoming light beams.

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Photonic Integrated Circuits: From Sensing and Telecommunication to Quantum Applications

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Photonic integrated circuits (PICs) are devices integrating multiple active and passive photonic components onto a single chip. They typically include elements for on-chip light generation, transmission, manipulation and detection. As established in electronic integrated circuits, which process electrical signals using integrated transistors, capacitors, resistors, diodes and interconnects, PICs employ integrated lasers, optical waveguides, phase-/amplitude-modulators, optical filters, and photodetectors to handle signals in the photonic domain. By using photons instead of electrons, PICs enable certain advantages in signal processing such as high-bandwidths/-speed operation and overall low transmission losses. Additionally, they demonstrate to be very well suited for the emerging field of quantum applications [1].

PIC concepts have so far emerged as key components for applications ranging from optical communication [1] to medical [2] and environmental sensing [3], and novel quantum technologies [1]. For targeting different wavelength ranges and functionalities, different material systems and technologies have been developed, such as silicon photonics as platform technology, InP for integrated actives like light sources and detectors, and SiN for ultra-low-loss waveguides. In recent years, the ability to realize miniaturized and integrated complex photonic systems has been significantly extended through significantly improved fabrication processes and the development and implementation of advanced heterogeneous and hybrid integration technologies and packaging solutions. They enable the combination of different material platforms on one common chip-scale carrier.

In this presentation we will discuss the state-of-the-art in PIC developments with a focus on the near-infrared (NIR) and mid-infrared (MIR) spectral range. This will also cover our recent developments and technical contributions to those fields. In particular, we want to show a novel NIR monolithic InP-based PIC transmitter for signal transmission and communication in the c-band around 1550 nm [1]. It is presented in Fig. 1(a) and utilizes an advanced PIC concept that includes DBR laser source, amplitude and phase modulators and optical attenuators for the generation and emission of single photons suitable for quantum key distribution (QKD) protocols. The presented QKD transmitter chip is used for discrete-variable (DV) time-bin encoded BB84 QKD with the goal to enable qubit generation rates of 100 MHz.

Other individual PIC elements for the 1550 nm spectral range are shown in Fig. 1(b) & (c), extending the available toolbox of components by adding optical phased arrays (OPA) in SiN technology for the use in light detection and ranging (LiDAR) [4] or by exploring the capabilities of Al(Sc)N for integrated grating couples, optical ring resonators and directional waveguide couples [5].

In contrast to that, Fig. 1(d) shows a monolithic MIR PIC in a lab-on-chip configuration that we successfully used for in-situ reaction monitoring of a protein [6]. It is based on quantum cascade (QC) technology and combines QC laser (QCL) and detector (QCD) with advanced MIR plasmonic waveguide technology [7]. We developed this technology further, by additionally implementing micro-mirror optics to enable more complex MIR PIC geometries (see. Fig. 1(e)) [8].

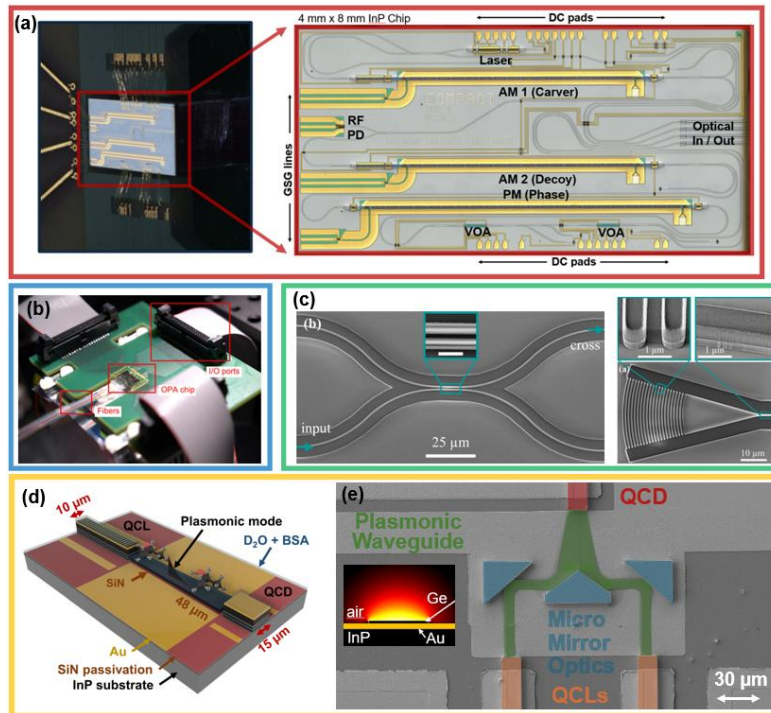


Figure 1: (a) InP transmitter PIC (PIC) for DV time-bin encoded BB84 QKD protocols [1].

(b) SiN-based integrated OPA at 1550 nm [4]. (c) Al(Sc)N integrated directional coupler and grating coupler [5].

(d) InP-based MIR monolithic lab-on-chip based on QC technology [6]. (e) Advanced InP-based MIR PIC demonstrating an integrated QC beam combiner [8].

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Electro-optic modulators and frequency combs in thin-film lithium niobate

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In recent years, thin-film lithium niobate (TFLN) has become an established platform for integrated photonics [1]: high-confinement waveguides, low propagation losses, and exceptional nonlinear properties make it very suitable for a broad range of integrated photonic devices and systems, as illustrated in Fig. 1. In this contribution, we will cover the basics as well as the state-of-the-art of electro-optic modulators and frequency combs based on the TFLN platform [2].



Figure 1: Thin-film lithium niobate has become an established platform for integrated photonics, allowing the integration of many different components on the same photonic chip.

Figure reprinted from Ref. [1].

One of the major practical applications has been the development of high-speed, low-voltage electro-optic TFLN modulators, routinely operating above 100 GHz at CMOS-compatible voltages [3]. These are based on the Pockels effect, where an applied electric field induces a change in the material's refractive index, allowing for efficient phase and amplitude modulators. Recent progress in optimizing such electro-optic devices includes maximizing the electric field overlap with the optical waveguide, along with advanced modulator electrode design for velocity matching, impedance matching, and low-loss broadband operation [4].

Beyond high-speed communication and data transmission, the strong electro-optic effect can be employed in a variety of other TFLN-based devices. One of the most important examples includes the electro-optic (EO) frequency comb [5], where a set of equidistant emission frequencies acts as a ruler in the frequency domain, useful for applications in spectroscopy, sensing, and communications, and establishing a coherent link between the optical and microwave regions of the electromagnetic spectrum. High-performance EO combs in TFLN combine optical resonators and traveling wave or resonant modulator electrodes, along with optimized microwave drive signals, to achieve high conversion efficiencies and broad spectral bandwidths [6,7].

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Quantum Photonic Integrated Circuits with Self-Assembled Quantum Dots

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Photonic quantum technologies provide a compelling platform for quantum information processing, leveraging single photons as robust carriers of quantum information and enabling long-distance communication through low-loss optical fibers. Among the most promising solid-state emitters, self-assembled InAs/GaAs quantum dots (QDs) have emerged as a mature and reliable technology for deterministic single-photon generation, operating in both near-infrared [1] and telecom wavelength [2] regimes. These sources enable a range of applications, from quantum key distribution [3] to distributed quantum computing, where indistinguishable photons and on-demand emission are essential.

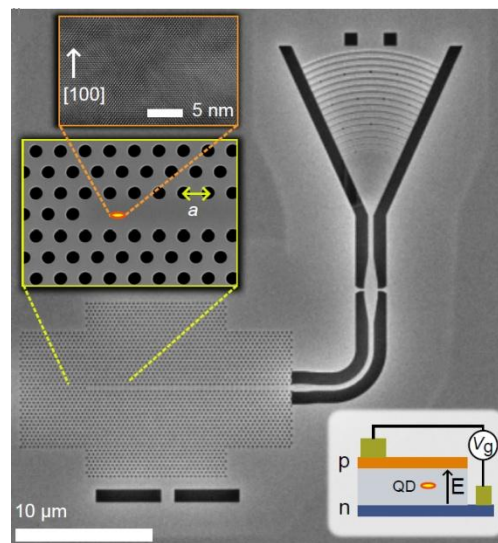


Figure 1: Waveguide-integrated gated telecom quantum dots. Scanning electron micrograph of a photonic crystal waveguide with full charge control through a p-i-n diode.

Embedding QDs within nanophotonic suspended waveguides, enables efficient coupling of emitted photons into guided modes, forming the foundation of integrated quantum photonic circuits (see Figure 1). Such waveguide quantum electrodynamics (QED) systems offer strong light-matter interaction, high collection efficiency, and low background noise, making them attractive for scalable on-chip quantum technologies. However, a fundamental limitation arises from the stochastic nature of the self-assembly process, which leads to random spatial positioning and spectral inhomogeneity of the quantum emitters. This disorder complicates the deterministic integration of multiple QDs and hinders the realization of large-scale, multi-emitter quantum photonic systems.

In this work, we present recent advances in addressing these challenges by introducing active control mechanisms based on nanomechanical devices [4] and photonic integrated circuits. By exploiting tuning via nanomechanical actuation, we demonstrate the ability to selectively modify



the emission properties of individual QDs, effectively compensating for spectral disorder and enabling resonance alignment between multiple emitters [5]. This approach introduces additional "tuning knobs" in waveguide QED platforms, allowing dynamic control over emitter–photon interactions and paving the way to scalable architectures.

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Microscale generation and control of nanosecond light by light in liquid crystals

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We demonstrate two examples of soft-matter photonic micro-integrated devices that operate exclusively on light: (i) 2D chip that integrates tunable cholesteric liquid-crystal (CLC) fluorescent dye micro-lasers and laser micro-printed polymer wave-guides¹, and (ii) 3D nematic liquid crystal droplet that is fluorescently labelled and submersed in water that connects to a set of tapered, laser micro-printed wave-guides². 2D planar chip with CLC micro-lasers is realized by direct laser writing (DLW) polymer multimode waveguides on glass with CYTOP optical insulation layer. The waveguides are connected to the DLW printed polymer scaffolds that host the CLC micro-lasers. 3D nematic droplet optical switch is realized by DLW printing tapered optical waveguides that form a robust scaffold, hosting a nematic droplet submersed in water. Whispering Gallery Mode lasing is initiated in the nematic micro-droplet by exciting the fluorescent dye through the waveguide-droplet robust coupler formed solely by surface tension. In both cases, we demonstrate the control of the liquid crystal's micro-laser emission by nanosecond optical pulses and introduce the concept of resonant stimulated-emission depletion (R-STED) to switch the light by light. The R-STED control of light signals in an optical cavity is achieved at very low light levels, which are typically several orders of magnitude smaller than conventional STED used in super-resolution imaging. This opens a new way to design an entirely new class of photonic integrated 3D devices that can be made both biodegradable and biocompatible with a rich variety of applications in medicine, wearable photonics, and logic circuits. We anticipate that soft-matter photonic circuits could outperform solid-state photonics in terms of a huge reduction in the number of production steps, and the use of non-toxic chemicals for their production.

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REGULAR PAPERS

**MATERIALS, TECHNOLOGY,
AND DEVICES**

On the maximum in the piezoelectric response of the solid solution $(1-x)\text{BiFeO}_3-x\text{BaTiO}_3$

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Bismuth ferrite (BFO) and barium titanate (BT) are two ferroelectric perovskites that form an extended solid solution [1]. This solid solution allows the stabilization of the perovskite structure of BFO, reducing the amount of detrimental secondary phases and its conductivity [2]. Being a lead-free material with a high T_c [3], it represents a good candidate for the substitution of the EU restricted lead-based ferroelectrics. The currently accepted structural evolution of this system was represented by Lee *et al.*, highlighting the presence of a morphotropic phase boundary (MPB) centered at $0.67\text{BiFeO}_3 - 0.33\text{BaTiO}_3$ ($x_{\text{BT}} = 0.33$) [3]. This MPB is believed to be the origin of the peak in the piezoelectric (and ferroelectric) properties of this solid solution, as it happens in many other systems. However, this behavior could be as well the result of an initial softening of BFO caused by BT addition either due to reduction of pinning sites and/or due to the induced relaxor behavior and then a non-ergodic-to-ergodic phase transition, both observed by independent research groups [4,5]. In this sense, the whole piezoelectric compositional evolution would be hypothetically dominated by the relaxor behavior progressively induced by adding BT to BFO.

In this work, dynamic converse piezoelectric experiments, coupled with extensive structural and electric characterizations are pursued on Mn-doped BFO-BT with the compositions ranging from 0.80 to 0.60 of BFO fraction, to uncover the phenomena underlying the performances of BFO-BT and the origin of the peak in the piezoelectric properties as function of composition. The converse longitudinal piezoelectric coefficient (d_{33}), the dielectric permittivity (ϵ_{33}) and their respective tangent of phase angles ($\tan\delta_p$ and $\tan\delta_d$) were obtained. The reversible (d_{33}^{init} , $\epsilon_{33}^{\text{init}}$) and irreversible (α_p and α_d) Rayleigh coefficients have been calculated, according to Rayleigh law for ferroelectrics, which has been applied to the dielectric response as well:

$$d_{33}' = d_{33}^{\text{init}} + \alpha \cdot E_0 \quad \epsilon_{33}' = \epsilon_{33}^{\text{init}} + \alpha \cdot E_0$$

where d_{33}' is the real part of longitudinal piezoelectric coefficient, ϵ_{33}' the real part of dielectric permittivity, and E_0 the driving field amplitude. The losses extrapolated at zero field ($\tan\delta_p^{\text{init}}$, $\tan\delta_d^{\text{init}}$) have been calculated as well. Preliminary data show that the relaxor transition may play a major role in the dielectric, piezoelectric and ferroelectric features of this system. In particular, the decrease of d_{33}^{init} for the compositions below 0.67 of BFO (Figure 1a, black), not followed by a decrease of $\epsilon_{33}^{\text{init}}$ (Figure 1b, black) or of the losses (Figure 1a and 1b, red). There are two possibilities to explain such behavior. First, at high BT content a contribution to the electrical response (permittivity) is observed that is not reflected to the same extent to the electromechanical response (piezoelectricity). Second, the behavior could also be attributed to the transition from non-ergodic to ergodic state, in which the polar nano-regions (PNRs) stop to retain the long-range ordering after the removal of E , contributing then only to ϵ . The asymmetric peak of α_d with respect to α_p ,

meaning that α_d (unlike α_p) does not drop to zero at higher BT content, is in accordance with this hypothesis (Figure 1c).

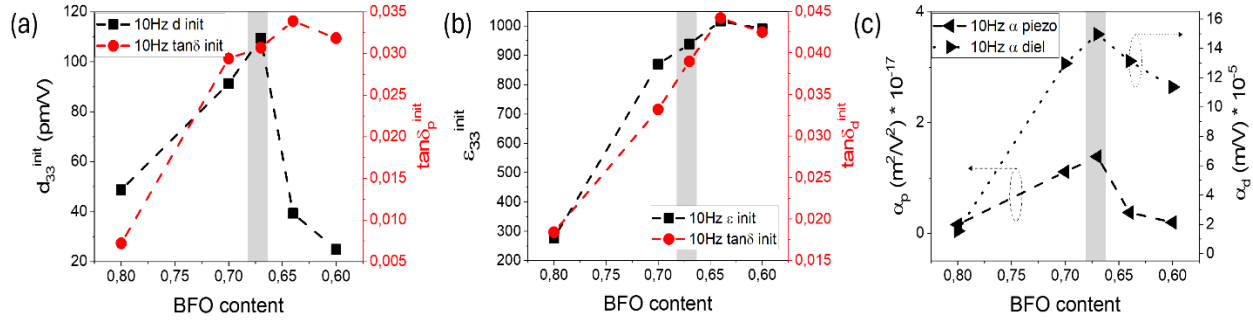


Figure 1: (a) converse d_{33}^{init} (black) and $\tan\delta_p^{init}$ (red), and (b) ϵ_{33}^{init} (black) and $\tan\delta_d^{init}$ (red), measured at 10Hz of driving frequency and from 1% to 15% of the coercive field E_c of each composition, as function of BFO content in BFO-BT. (c) α_p and α_d calculated for the highest driving field, being 15% of E_c . The shaded region indicates the MPB as reported in the literature [3].

Determining the nature of the transition occurring at $x_{BT} = 0.33$ will increase the knowledge of this ferroelectric solid solution, allowing more effective tailoring of its properties as well.

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Utilization of Focused Ion Beam (FIB) for Cross-section and Transmission Electron Microscopy analyses of Semiconductors and Chips

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Focused Ion Beam technology is in principle similar to scanning electron microscopy (SEM), but instead of electron beam it utilizes ion beam (common sources include elements Ga, He, Ar, Xe). It can be used only as analytical tool similar to SEM, however due to much larger energies of ion it is mostly used as very precise milling tool at micro-to-nano scale with possible deposition of various elements (e.g., Pt, W, C) using ion gas injection technology. FIB primary use in electronic industry was for precise manipulations of circuits in chips, but in recent decade it's use has expanded to conduct site-specific cross-sections of chips that can be analyzed with SEM equipped with energy-dispersive X-ray detector (EDXS) to search for defects and changes in chemical composition. Furthermore, site-specific thin slices known as lamellae can be cut from the sample in order to conduct nanoscale analyses with TEM. These include observing structure, defects and chemical composition of chips at nanoscale level up to atomic resolution in order to facilitate identifying manufacturing defects, short-circuits, changes in compositions and other phenomena occurring at the nano-scale.

Lamella preparation of chip sample for TEM analysis generally consists of four steps. The first step is to identify the desired area of a sample to be analyzed. This is usually done using SEM, which most modern FIB system are already equipped with. After locating the desired area, a thin, protective layer of Pt, W or C is deposited via GIS system. This also marks the size of the lamella, which is usually 10-20 μm long and can be cut up to 10 μm in the sample. The layer provides protection of the sample against highly energetic ion beam used in the upcoming steps (figure 1 a). Second step is to use 9-60 nA current of ion beam at 30 kV to etch the trench around the protective layer which effectively makes a cross-section of the area. Therefore, after the second step, SEM-EDXS analysis of the cross-section can be done (figure 1 b). In the third step, lower currents of ion beam (9 nA to 80 pA) at 30 kV are used to cut the lamella out of the sample and transfer it to the appropriate TEM grid using micromanipulator needle (figure 1 c). Lamella is then welded onto the grid using GIS (figure 1 d). Lamella on grid can then be thinned using progressively less energetic ion beam to achieve electron-transparency (usually 100-10 nm thickness). Usually, the current of the ion beam at this step is lowered from 0.8 nA to 20 pA and voltage from 30 kV to 1 kV for the final polishing of the lamella. Lower energies induce much less damage to the sensitive lamella and can be used to remove any induced amorphization that may occur during second and third step of the lamella preparation with FIB.

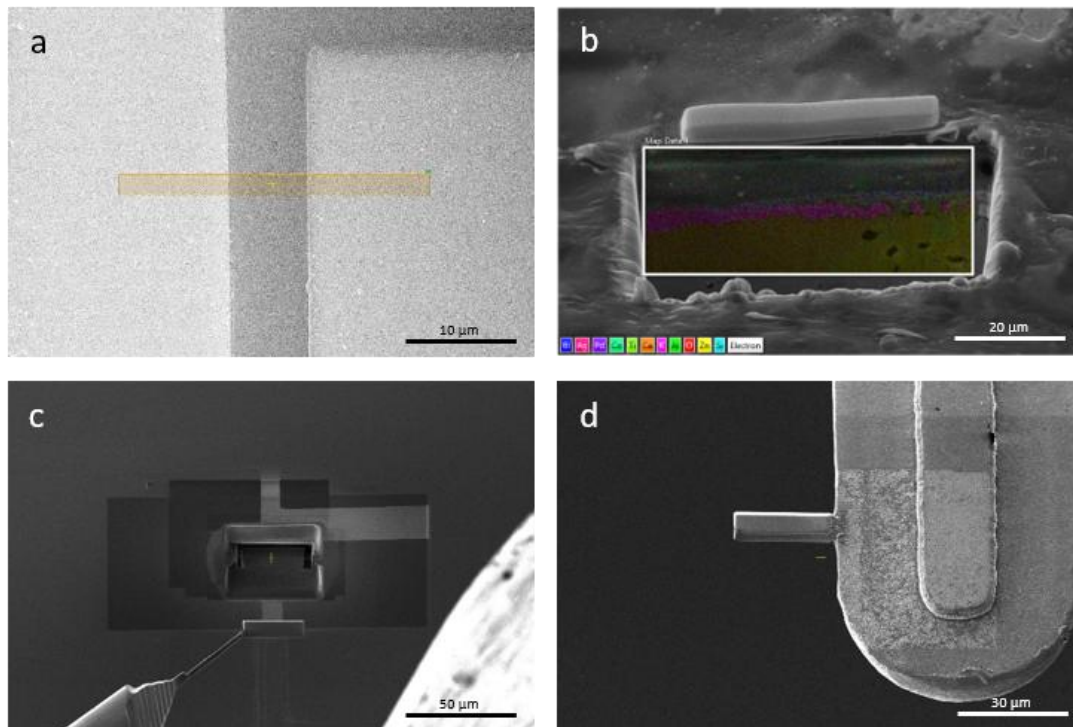


Figure 1: FIB is equipped with SEM and each step of lamella preparation can be observed and snapshotted using SEM. a: Orange rectangle on Al circuit on silicon wafer marks the area of the lamella takeout. Pt protective layer is deposited. b: After etching the trench around Pt layer, SEM-EDXS analysis can be conducted and elemental map of the cross section can be done as shown on the image. c: Micromanipulator needle with lamella attached to it right after it has been lifted from the sample. Trench holes and circuit can be seen. d: lamella welded onto TEM grid.

Multiscale analysis of a commercial and lab-fabricated SOFC

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Existing fossil-fuel power units should be replaced with more efficient and environmentally benign alternatives, such as fuel cells. They are electrochemical devices consisting of two electrodes, an anode and a cathode, separated by an electrolyte. The oxidation and reduction reactions at the fuel cell's electrodes convert chemical energy into electrical energy in an ecologically indisputable manner, making fuel cells a viable alternative to current energy systems. Solid Oxide Fuel Cells (SOFCs) are high-temperature fuel cells, and their operation is the least sensitive to fuel quality among fuel cell types. They offer fuel flexibility, almost zero emissions, and facilitate the transition to renewable energy sources [1].

The objective of our work was to fabricate an anode-supported button SOFC using tape casting and screen printing (further on referred as JSI-SOFC), test its electrical properties and performance, and compare it to a commercial SOFC (XTAL-SOFC, XTAL d.o.o, Slovenia).

The anode was produced by tape casting a suspension of nickel oxide and yttrium oxide stabilised zirconium oxide (NiO-YSZ ((Y₂O₃)_{0.08} (ZrO₂)_{0.92}) mixed in the 40:60 mass ratio. The tape-cast sheets were laminated to the anode thickness of 400 μm and cut into desired shapes. The remaining elements of the fuel cell, the YSZ solid electrolyte, the lanthanum strontium cobaltite ferrite (La_{0.6}Sr_{0.4}Co_{0.2}Fe_{0.8}O_{3-δ}, LSCF) cathode and the protective layer of gadolinium oxide doped cerium oxide (Ce_{0.9}Gd_{0.1}O_{1.95}, GDC) were screen printed. The JSI-SOFC was sintered in multiple steps, which can be seen in Figure 1.

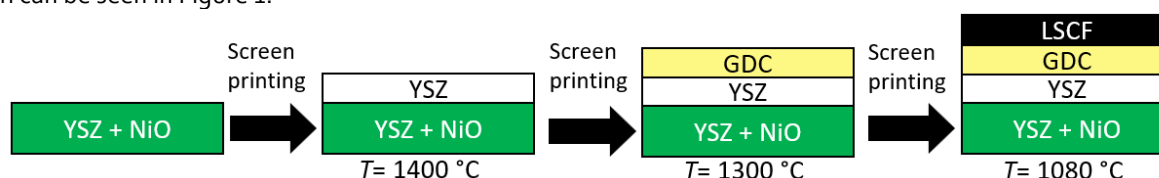


Figure 1: Fabrication process of a JSI-SOFC sample. YSZ + NiO anode was used a substrate and YSZ electrolyte was screen printed on it and sintered at 1400 °C. After sintering, GDC barrier layer was printed on top of the YSZ and sintered at 1300 °C. Lastly, LSCF cathode was printed on top of the GDC and sintered at 1080 °C.

Focused ion beam – scanning electron microscopy (FIB-SEM) and energy dispersive X-ray spectroscopy (EDXS) were used to analyze the samples before and after operation.

Current – voltage – power (I-V-P) measurements were performed on the samples at 700 °C. Humidified H₂ and synthetic air were used as fuel on the anode and cathode sides, respectively. Electrochemical impedance spectroscopy (EIS) was performed in the frequency range of 0.1 Hz to 100 kHz under the same conditions. The Nyquist plots were fitted using an open-source program called DearEIS [2].

JSI-SOFC and XTAL-SOFC FIB-SEM x-cut cross-sections can be seen in Figure 2 a) and b) respectively. The porosity of the JSI-SOFCs barrier and cathode layers is higher than that in the XTAL-SOFC (see yellow and black lines, respectively). The thicknesses of individual layers also differ, with the JSI-SOFC cathode and electrolyte thinner than those of the XTAL-SOFC (~7 μm compared to ~12 μm for the cathode and ~7 μm compared to ~12 μm for the electrolyte).

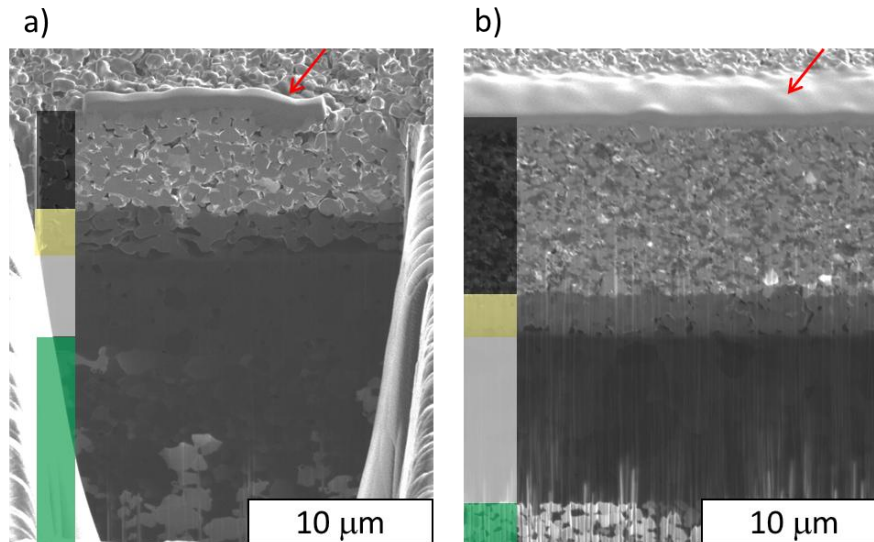


Figure 2: FIB-SEM x cut cross-section of a) JSI-SOFC button cell, b) XTAL-SOFC button cell. Pt was used as a protective coating before cutting the sample (red arrow). JSI-SOFC shows visible porosity in the barrier layer, compared with the same layer in the XTAL-SOFC (marked in yellow). The porosity in the cathode layer is also visibly higher in the JSI-SOFC (marked black). The colours on the left side of the microstructures match the color scheme presented in Figure 1.

IVP and Nyquist plots of the cells were measured at 700 °C. The JSI-SOFC exhibits a lower open circuit voltage (0.81 V) than XTAL SOFC (1.09 V), a lower peak power density (0.03 W/cm² to 0.23 W/cm²), and a steeper voltage drop with increasing current density compared to the XTAL-SOFC. This performance gap is evident in the impedance spectra, as the XTAL-SOFC has an area specific resistance (ASR) of 1.18 Ωcm², meanwhile the JSI-SOFC has an ASR of 8.41 Ωcm². The observed performance difference between the cells can be attributed to several factors related to the microstructure of the individual cell components [3][4].

Future work will focus on optimising the fabrication of the JSI-SOFC to reduce porosity in the barrier layer. FIB tomography will be used to map the porosity distribution in the cathode and anode layers. The mapping will be an input for a finite element model which will be constructed to verify the experimental results and provide guidelines for improving performance.

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From SEM-Induced Carbon Contamination to Nanostructure Growth and Near-Surface Transformations

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Abstract Summary. Scanning electron microscopy (SEM) and energy-dispersive X-ray spectroscopy (EDS) are indispensable for nanoscale characterization, but in beam-sensitive metal chlorides the electron beam can become a local processing source rather than a passive probe [1,2]. Here, crystalline gold trichloride (AuCl_3) is used as a model system to examine how low-energy SEM irradiation drives coupled surface growth and near-surface transformation during analysis. AuCl_3 crystals were irradiated in spot mode at accelerating voltages from 1 to 30 kV and exposure times up to 1080 s. Operando SEM-EDS was combined with focused ion beam cross-sectioning, theoretical energy-deposition models, and Monte Carlo simulations [1]. Electron irradiation produced carbon nanopillars on the surface through the dissociation and polymerization of hydrocarbons. Their lateral growth decreased with increasing accelerating voltage, while vertical growth became more pronounced at higher electron energies, indicating a strong role of secondary and backscattered electrons [3]. At the same time, the near-surface AuCl_3 decomposed below irradiated regions, producing chlorine loss, Au nanoparticle formation, and voids. These coupled transformations show that SEM-induced carbon contamination is not only an analytical artefact but may also become a controlled nanostructure-forming route, provided that the accompanying subsurface damage is understood.

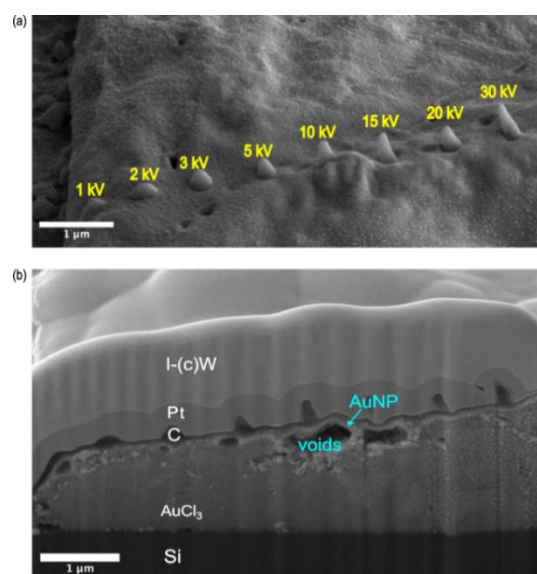


Figure 1.: a) growth of C-pillars on the surface and near-surface transformation of beam-sensitive AuCl_3 under low-energy SEM irradiation

Explanatory. The upper part of Fig. 1 presents the surface-growth component of the process. After SEM spot irradiation from 1 to 30 kV, carbon deposits appear as localized nanopillar-like structures on the AuCl_3 surface. This carbon accumulation originates from electron-induced dissociation and polymerization of residual or adsorbed hydrocarbons in the SEM chamber, a well-known source of electron-beam-induced contamination [2]. In the present case, however, the deposits do not remain as a simple contamination layer but develop into distinct three-dimensional carbon nanostructures. The full dataset shows that pillar growth depends strongly on both irradiation time and accelerating voltage. Lateral growth is faster at lower accelerating voltages and tends toward saturation, while vertical growth becomes more pronounced at higher beam energies. This behavior is consistent with a mechanism in which incident electrons initiate the process, secondary electrons directly promote hydrocarbon dissociation near the irradiated region, and backscattered electrons contribute indirectly by generating additional secondary electrons [3]. Therefore, the same phenomenon normally considered a SEM artefact can be reframed as a controllable electron-beam-induced nanostructuring route. The lower part of Fig. 1 shows the hidden near-surface transformation below the carbon structures. FIB cross-sectioning reveals that the AuCl_3 crystal is modified beneath the irradiated surface: voids form inside the near-surface region, while Au nanoparticles appear as a result of Au–Cl bond breaking, chlorine loss, and local gold redistribution. Operando EDS confirms that the chemical signal changes during irradiation, meaning that prolonged SEM-EDS acquisition can alter the composition it is intended to measure [1]. Thermal calculations show that beam heating is insufficient to explain the observed void formation. Instead, theoretical energy-deposition analysis and Monte Carlo simulations support a radiolysis-driven mechanism, where deposited electron energy promotes AuCl_3 decomposition and mass loss. The central message is therefore not only that AuCl_3 is beam sensitive, but that SEM irradiation produces two coupled outcomes: carbon nanostructure growth above the surface and radiolytic material transformation below it. This coupling defines the limits of reliable SEM-EDS analysis and suggests a route toward controlled near-surface nanoengineering in beam-sensitive metal chlorides

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Measured and simulated ion number density in low pressure argon RF plasma

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To predict the behaviour of the physics of plasma, COMSOL Multiphysics simulation is often used in the plasma physics community. In this work we compare the simulation results of axial profile of number density of charged ions in argon low pressure radio frequency plasma to physical results measured with the Langmuir probe. There is an obvious discrepancy between the results, although the shape of the curve is similar, as is the order of the magnitude of the number density of ions. The future work remains to adjust the parameters of the simulation to fit the measured results better in order to increase the accuracy of the simulation for future cases.

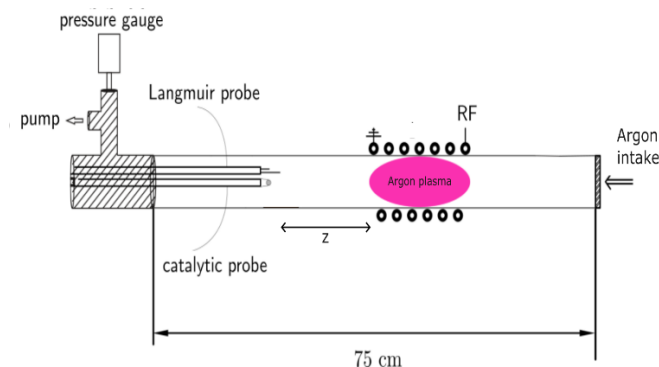


Figure 1: The experimental plasma setup and the position of the Langmuir probe in the reactor.

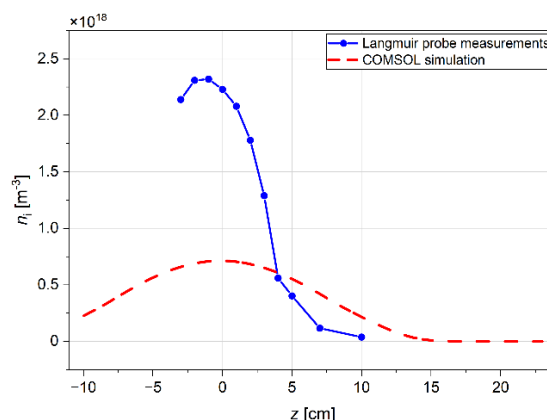


Figure 2: The results from Langmuir probe measurements (blue) and the simulated results in COMSOL (red) of ion number density at different distances from the center of the coil.

PLASMA-SURFACE ENGINEERING OF Ti_2C MXENE FOR ENERGY STORAGE APPLICATIONS

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The growing demand for clean and sustainable energy solutions, driven by rapid industrialization and rapid consumption of fossil fuels, has intensified the efforts to develop more efficient energy storage systems (ESS). Among these, supercapacitors (SCs) have emerged as leading candidates, offering high power density, fast charge-discharge cycles, low self-discharge, and stable performance. Despite these advantages, their broader application remains limited by relatively low energy density, which is primarily influenced by electrode material properties. Among emerging electrode materials, MXenes - a new category of two-dimensional transition metal carbides and nitrides - have demonstrated strong potential as electrode materials for SCs because of their high electrical conductivity, chemical tunability, and mechanical strength [1]. In this study, we evaluate the performance and electrochemical properties of Ti_2C MXene synthesized from the Ti_2AlC MAX phase using ammonium bifluoride as an electrode for SCs. Compared to conventional HF etching, this approach offers a safer, more environmentally friendly alternative, minimizing toxic byproduct formation while improving the surface properties of Ti_2C MXene. Later on, the accordion-like layered MXene was subjected to mild plasma treatment to increase the number of electroactive sites. Ti_2C MXene was later functionalized via sulfur plasma treatment to effectively replace -F termination groups on the surface of the MXene with S-containing groups. The incorporation of sulfur introduces additional redox-active sites into MXenes, which enhance their pseudocapacitance, strengthen electrode-electrolyte interactions, and reduce charge-transfer resistance [2]. The prepared S-MXenes electrodes exhibit a remarkable increase in capacitance, achieving 733 F g^{-1} at a current density of 1 A g^{-1} with high electrochemical stability over 10000 cycles. Furthermore, an asymmetric full cell device was fabricated using the S-MXene, revealing a stable electrochemical performance suitable for long-term use. Employing such plasma-based techniques for the fast and green surface engineering of MXenes highlights the significance of plasma-surface engineering to tailor advanced electrode materials with enhanced energy storage performance for SCs.

Key words: Energy storage, supercapacitors, MXenes, plasma-surface engineering, surface functionalization, cycling stability.

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Coaxial Core-Shell Carbon/Tin Sulfide Nanohybrids for High-Performance and Durable Supercapacitor Electrodes

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As next-generation high-power energy storage systems, supercapacitors demand electrode materials capable of rapid charge transfer, high power density, and exceptional long-term electrochemical stability. Among various candidates, hybrid architectures combining electric double-layer capacitance with pseudocapacitive behavior have emerged as an effective strategy to enhance both energy storage capability and cycling durability. In this study, we report the fabrication of a coaxial core-shell carbon-tin sulfide (SnS@VCN) nanohybrid electrode through a rapid plasma-assisted dry synthesis technique. The approach enables the conformal growth of layered SnS nanosheets onto vertically aligned nanocarbon (VCN), forming a highly conductive and mechanically stable hierarchical architecture. The unique plasma-engineered interface between SnS and the carbon scaffold promotes efficient electron transport, accelerates ion diffusion, and mitigates structural degradation during repeated charge-discharge processes. Benefiting from these synergistic effects, the binder-free SnS@VCN electrode delivers a high specific capacitance of 577 F g⁻¹ (242 C g⁻¹) at a current density of 3 A g⁻¹ and maintains 72% of its capacitance even at a high current density of 12 A g⁻¹. Remarkably, the electrode exhibits outstanding cycling durability, achieving 115% capacitance retention after 10,000 charge-discharge cycles, indicating progressive electrochemical activation and superior structural integrity. To evaluate its practical applicability, an asymmetric supercapacitor device based on SnS@VCN//activated carbon (AC) was assembled. The device demonstrates a specific capacitance of 17.8 F g⁻¹ together with exceptional cycling performance, retaining 140% of its initial capacitance after 5,000 cycles. The enhanced electrochemical behavior is attributed to the combined advantages of the hierarchical core-shell morphology, conductive carbon framework, and plasma-tailored interfacial engineering, which collectively overcome the sluggish kinetics and poor cycling stability commonly associated with conventional battery-type electrodes. This work presents a scalable, environmentally friendly, and binder-free route for constructing advanced metal sulfide-carbon nanohybrids and highlights the strong potential of plasma-assisted interface engineering for developing ultra-stable, high-rate electrode materials for future supercapacitor technologies.

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Localized Surface Plasmon Resonance Enhanced Laser Lithography on Highly Insulating Substrates

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Abstract Summary

This work presents a novel approach to maskless, direct write lithography using a low power laser by decoupling nanoscale heat generation from macroscopic substrate dissipation. Using the localized surface plasmon resonance effect in silver nanoparticles on highly insulating nanostructured substrates, we achieve very high, localized temperature increase to induce precise melting and solid state dewetting using a low power continuous wave 488 nm laser. Combining experimental nanofabrication of nanoparticles with COMSOL multiphysics simulations and machine learning, we study the nonlinear, stochastic thermal thresholds of this process. This establishes a predictable, energy efficient nanomanufacturing technique for printed flexible electronics and advanced printed microcircuits.

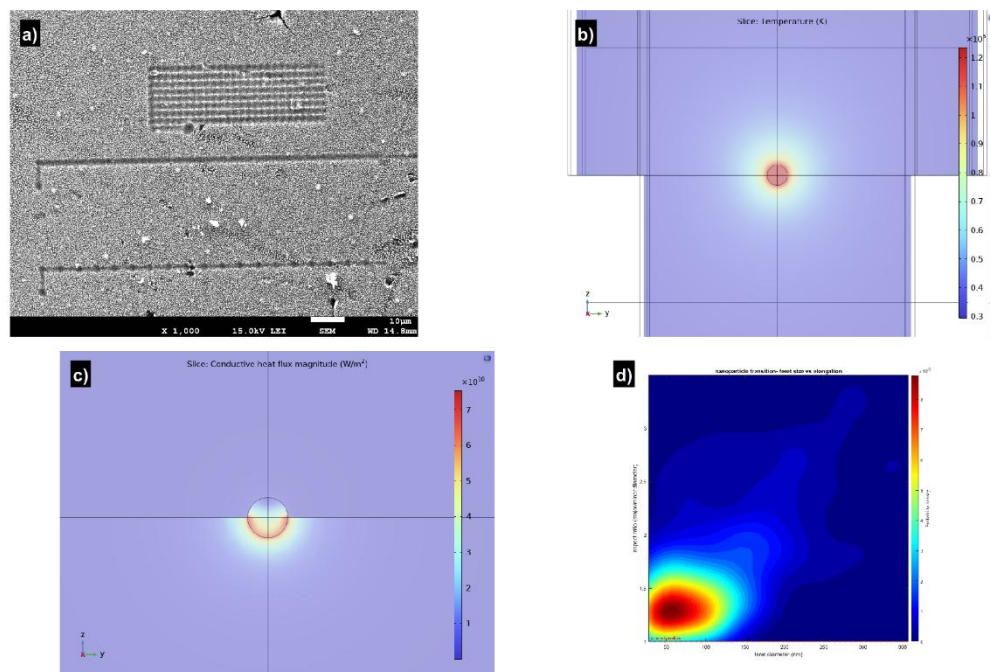


Figure: (a) SEM image of visible, laser melted silver nanoparticle tracks ablated onto a nanostructured alumina substrate, (b) and (c) COMSOL simulations of temperature and heat dissipation showing extreme localized heating (~ 1300 K) of a 30 nm Ag nanoparticle on nanostructured alumina. (d) KDE heatmap of aspect ratio versus feret diameter tracking the morphological evolution of Ag nanoparticles.

Explanatory text: Aim, scientific innovation and results

To tackle the resolution limits of conventional lithography and the heat dissipation issues of maskless direct writing by laser, we experimentally used a complex material system consisting of four substrates, namely:

1. Commercially available flat, conductive, doped Silicon,
2. 300 nm thick flat Silicon Oxide on Silicon,
3. 300 nm layer of nanostructured, grass-like alumina layer on 3 inch Silicon, and
4. 600 nm layer of nanostructured, vertical carbon nanowalls on SiO₂ substrate.

Sputtering all four substrates with silver, followed by global furnace annealing at 400-500 °C for 5 minutes induced solid state dewetting and diffusion of silver, subsequently followed by nucleation of silver nanoparticles. Next, shining a continuous wave, 5 mW, 488 nm laser of a spot size of about 1 micron on the resulting nanoparticles exploited their LSPR effect to generate heat, and then leveraged the nanoscale thermal bottlenecks from the nanostructured substrates (e.g.- Kapitza resistance, reduced thermal conductivity) to confine heat within the discrete nanoparticles. This synergistic, dual effect effectively allows us to develop a unique, tunable, localized, maskless lithography technique with the ability to switch between very high localized temperature (ablation) regime and more controlled, moderate temperature (sintering) regime.

To theoretically describe and understand mechanisms of behaviour in our system, Multiphysics modules of COMSOL were used, which replicate experimental results across three substrates:

1. Nanostructured Alumina: Modeled via Bruggeman SEMA approximation (91% void fraction calculated). Optically transparent with low thermal conductivity, forcing 100% absorption into the Ag nanoparticle. Result: ~1,300 K temperature spike, triggering violent liquid melting and ablation.
2. Vertical Carbon Nanowalls: Modeled via Bruggeman SEMA approximation (85.5% void fraction calculated). The substrate volumetrically absorbs the laser energy, similar to a broadband absorber. Result: ~700 K temperature spike, triggering 1D solid state dewetting without ablation.
3. Silicon: A well known infinite heat sink, massive intrinsic thermal conductivity on Si rapidly dissipates heat. Result: ~1.7 K rise, hindering morphological transformation.

A strong ablation effect is noticed with the nanoparticles nucleated on the nanostructured alumina substrate upon laser shining, whereas a weaker, sintering-like effect is visible on the carbon nanowall substrate using the same laser parameters, while no visible effects are observed for the flat substrates.

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THIN AND THICK FILMS

0.7Pb(Fe_{0.5}Nb_{0.5})O₃–0.3BiFeO₃ thick films for energy storage applications

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(1-x)Pb(Fe_{0.5}Nb_{0.5})O₃-xBiFeO₃ (PFN-100xBFO) ceramics exhibit from ferroelectric, relaxor to antiferroelectric behaviour. While studies on PFN-100xBFO bulk ceramics have been reported, PFN-100xBFO thick films have not yet been explored. Thick films can withstand higher electric fields compared to bulk ceramics and are key to the miniaturization of electronic components.

In this work, PFN-30BFO thick films were prepared for the first time. The PFN-30BFO powder was synthesized by mechanochemical approach and mixed with an organic vehicle composed of alpha-terpineol, 2-2-butoxy-ethoxy-ethyl acetate and ethyl cellulose in a mass ratio of 60:25:15. The thick-film paste was screen printed onto gold-coated Al₂O₃ substrates. To achieve films with optimal functionality, they were sintered for 2 h in an oxygen atmosphere at three different temperatures, namely 800 °C, 850 °C and 930 °C. The films annealed at 800 °C had the smallest grain size (Fig. 1a) and low electrical conductivity, resulting in the highest dielectric breakdown strength among the investigated samples. This makes the films promising for use in high-voltage electronic devices. Therefore, the energy storage properties of the PFN-30BFO thick films sintered at 800 °C were determined from the polarization versus electric field hysteresis loop (Fig.1b). The recoverable energy storage density of the films reached 2.8 J·cm⁻³ at 400 kV·cm⁻¹ and the energy storage efficiency was determined to be 79 % at 400 kV·cm⁻¹. The favourable energy storage performance of the PFN-30BFO thick-film samples demonstrates their potential for use in energy storage applications.

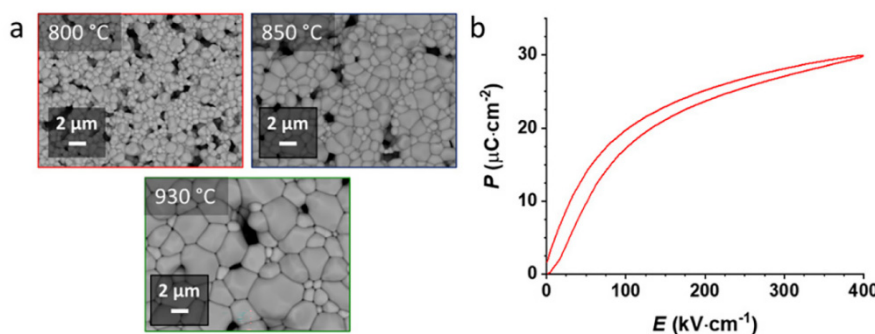


Fig. 1 (a) SEM microstructure of the surface of the thick films. (b) *P*–*E* hysteresis loop of the thick film annealed at 800 °C, used to calculate energy storage properties.

Optimization of Energy Storage Properties of Antiferroelectric Thick Films Through MLCC Architecture

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In recent years there has been an ever-increasing demand for compact and sustainable pulsed-power systems that has ignited strong interest in dielectric capacitors. Materials such as lead-free antiferroelectric (AFE) perovskites, particularly sodium niobate (NaNbO_3) derivatives, are considered attractive candidates due to their electric-field-induced phase transition, which can offer high energy density together with low thermal drift of the permittivity and minimal hysteretic losses. However, to truly grasp the maximum potential of those materials, the best strategy currently known is to translate those bulk materials into thinner layers that can be stacked with internal electrodes to create a multilayer ceramic capacitor (MLCC). This architecture can allow industrials to obtain very high dielectric breakdown field in a small component. But despite the advantages of such an architecture, transferring the bulk properties into the final MLCC device is quite often a big challenge, creating a barrier between academic research and industrial application. It is therefore essential to bridge this gap by achieving functionally thick active layers while preserving high crystalline quality, good density, and low volumetric defect density which becomes increasingly difficult as the layers are thinned down to few tens of micrometers.

This contribution reports on the processing of thick NaNbO_3 -based ceramic layers by tape casting, and their integration into a MLCC device. The suspension properties for tape casting were optimized to achieve appropriate stability of the particles in the organic solvent, suitable rheological behaviour, and thermal decomposition of organic phases, ensuring effective casting, and formation of defect-free green tapes. The chemical composition of the powder and sintering of green-tapes have been studied in order to optimize the energy storage properties of the ceramic structures and MLCC device, such as the permittivity, the thermal drift or the dielectric breakdown field. This contribution therefore reports on our latest advances in methodology on the tape-casting parameters of NaNbO_3 -based thick films, together with ongoing structural, microstructural characterization as well as preliminary dielectric measurements and polarization behavior of the multilayer device. We will present the challenges of stabilizing a strong antiferroelectric response in thick-film geometries that approach the one measured in their bulk material form.

Preparation of $\text{Pb}(\text{Sc}_{0.5}\text{Ta}_{0.5})\text{O}_3$ thick films by powder aerosol deposition

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$\text{Pb}(\text{Sc}_{0.5}\text{Ta}_{0.5})\text{O}_3$ (PST) is a perovskite oxide where the Sc^{3+} and Ta^{5+} cations occupy the B-sites of the crystal structure. These cations can be randomly positioned over the B-sites or assume a nearly 1:1 B-site ordered arrangement. The degree of cation ordering is described by the ordering parameter Ω , which varies from 0 (i.e., complete disorder) to 1 (i.e., complete order)[1]. B-site ordered PST undergoes a sharp phase transition from a pseudo-cubic paraelectric state to a rhombohedral ferroelectric state near room temperature (RT). This is accompanied by a larger maximum polarization of the ordered material. On the other hand, for its disordered counterpart, the transition is broader and shifted by approximately 15 °C to lower temperatures[2], [3]. A room-temperature phase transition and enhanced polarization makes B-site order PST particularly attractive for pyroelectric sensing and electrocaloric (EC) solid-state cooling near RT[4], [5].

Functional films enable the miniaturization of sensors and cooling devices. In EC applications, micrometer-thick films can outperform thinner films by exchanging more heat per cycle due to their larger active mass. However, the preparation of B-site ordered PST thick films remains a challenge, as high degree of ordering is achieved by thermal treatments at temperatures near or above 1000 °C for long time periods (e.g., 48 hours)[6]. Such processing conditions limit the compatibility of the film with the temperature-sensitive substrate and promote chemical reactions at the substrate–film interface. To overcome these limitations, powder aerosol deposition (PAD) offers a relatively simple and fast method that enables the direct preparation of ceramic thick films onto a variety of substrates at RT. In this process, the dry powder is deposited at high velocity directly onto the substrate, achieving RT consolidation of the film[7].

In this work, we prepared B-site ordered PST thick films by the PAD method. To prepare the B-site ordered PST films, we developed a new procedure as schematically shown in Figure 1a. The bulk ceramic pellets with the ordering degree of $\Omega = 0.82$ were milled and thermally treated to obtain the PST powder suitable for PAD. The deposition was performed onto stainless steel (SS), the standard and most commonly used substrate for this process. After deposition, the films were annealed at 600 °C for 1 hour in air to relieve the thermal stresses developed during the PAD process. The films exhibited a dense microstructure and excellent adhesion to the substrate. The high degree of B-site ordering was maintained in the deposited films ($\Omega = 0.78$), as shown in Figure 1b. The annealed films presented maximum relative permittivity of 225 at 1 MHz and RT, and maximum polarization of 38 $\mu\text{C}\cdot\text{cm}^{-2}$ at 850 $\text{kV}\cdot\text{cm}^{-1}$ and RT (Figure 1c). In conclusion, in this work, we prepared aerosol-deposited PST thick films with high B-site cation ordering, which has potential for future use in microelectronics.

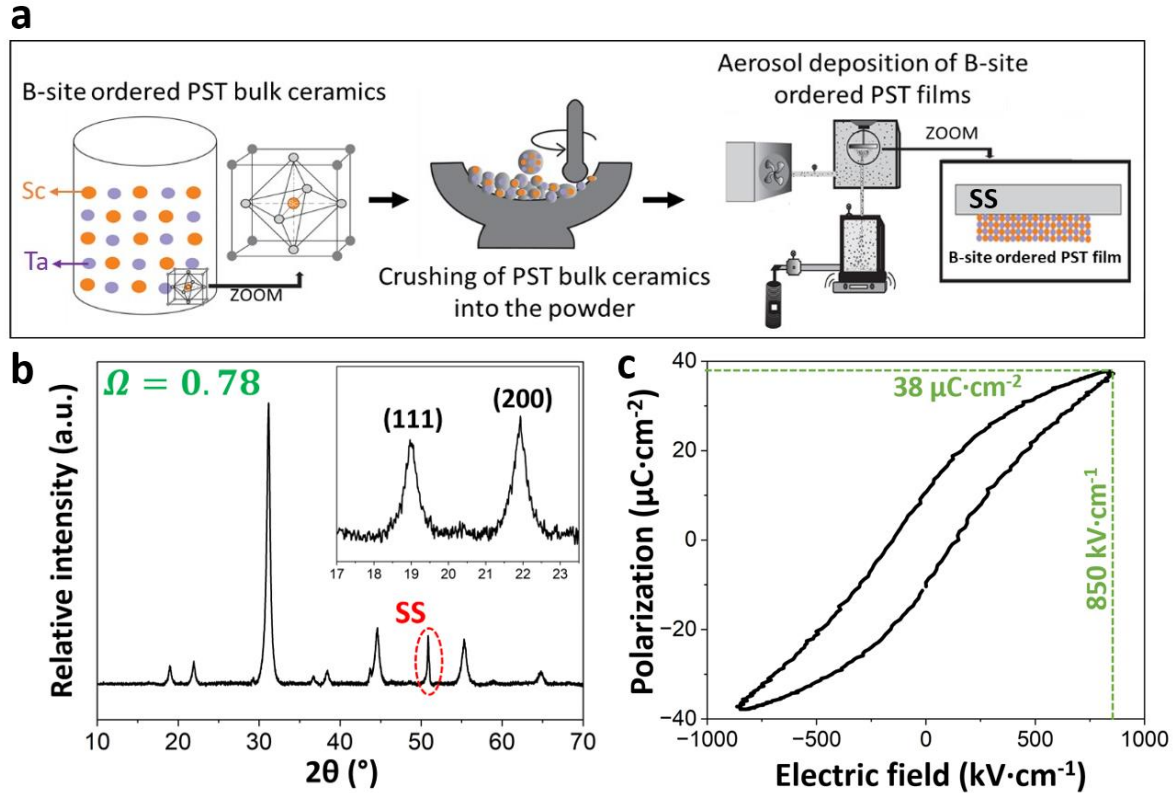


Figure 1: (a) Preparation procedure of B-site ordered PST thick films by the PAD method. (b) XRD spectrum of the B-site ordered PST film. The intensities of the (111) and (200) reflections reported in the zoom-in inset were used to calculate the order parameter Ω . (c) Polarization-electric field loop measured at RT of the annealed B-site ordered PST film with an applied field of $850 \text{ kV}\cdot\text{cm}^{-1}$.

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Fabrication of polyimide thick films via powder aerosol deposition

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Although solution-based, thermally assisted, and vapor-phase techniques are widely used for polymer film fabrication, the preparation of dense polymer thick films remains challenging because solution-based and thermally assisted routes often involve solvents or post-deposition curing at elevated temperatures, whereas vapor-phase techniques are generally better suited to thin-film deposition. In this work, we investigate powder aerosol deposition (PAD) – a room-temperature, solvent-free technique, traditionally used for the deposition of ceramic materials [1] – as a novel approach for fabricating pristine polyimide thick films. We examine how powder pre-treatment affects the particle size and morphology of the powder and, consequently, the deposition behavior, microstructural, mechanical and dielectric properties of PAD-deposited polyimide thick films. Besides commercially available polyimide powder, powder was pre-treated by wet milling at 100 rpm, and dry milling at 100 rpm and 200 rpm, resulting in four different powders. PAD deposition was performed on gold-coated glass substrates under identical condition for all powders. As-deposited polyimide thick films were characterized from macroscopic to micro- and nanoscale using various techniques. Polyimide films from raw and wet-milled powders exhibit high deposition rates (up to 6.43 mm³/min), thicknesses in the range of ten μm, dense and uniform homogeneous microstructures, and enhanced dielectric and mechanical properties ($\epsilon_r \sim 8\text{--}9$, $\tan \delta < 0.017$, and $E \sim 3.1$ GPa). In contrast, films prepared from dry-milled powders showed inhomogeneous microstructures with voids and holes, low deposition rates, reduced dielectric permittivity ($\epsilon_r \sim 4.0$), and lower Young's modulus ($E \sim 2.4$ GPa). Differential scanning calorimetry and Fourier-transform infrared spectroscopy confirm that neither milling nor PAD itself alters the chemical structure of polyimide powders and films. These results demonstrate that optimized powder pre-treatment is critical for successful PAD of polymer thick films and highlight the potential of PAD-deposited polyimide as a room-temperature, solvent-free route to dielectric, insulating, and passivation layers for flexible and hybrid microelectronic applications.

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Ascorbic Acid-Assisted Hydrothermal Growth of ZnO Films for Functional Semiconductor Applications

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Zinc Oxide (ZnO) is a widely studied bandgap semiconductor owing to its superior optical characteristics and chemical stability, making it attractive for film electronic and optoelectronic applications. Controlled semiconductor film growth by low-temperature and cost-efficient processing techniques represents a challenge in the context of scalable device fabrication.

In the present study, the deposition of ZnO thin films is achieved by means of the hydrothermal method conducted at a low temperature of 90 °C, using zinc nitrate solution containing different concentrations of ascorbic acid as an environmentally benign growth medium.

The effect of ascorbic acid concentration on the formation of the crystalline structure and functional performance of deposited films has been carefully studied. Scanning electron microscopy (SEM) studies show that ascorbic acid significantly influences the crystallization conditions, allowing the fabrication of continuous homogeneous semiconductor thin films under a small concentration range (3 mM).

For improving structural stability and increasing film functionality in terms of the electronic materials, thermal post-annealing (600 °C for 2 hours) has been applied. The microstructure and surface properties of both as-deposited and annealed samples have been studied, proving the effectiveness of this treatment.

Overall, the current research emphasizes the importance of the hydrothermal growth method assisted by green additives as an affordable and controllable technique for the preparation of functional thin films based on oxide semiconductors.

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WORKSHOP ON INTEGRATED PHOTONICS

Design and Characterization of Low-Loss Integrated Photonic Components and Interfaces

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Photonic integrated circuits (PICs) combine a large number of optical components and interfaces on a single chip. Increasing the complexity and up-scaling PIC based systems also brings stringent performance requirements for each individual optical component and interface. Since PICs are often combined with external fibers, light sources, detectors and heterogeneously integrated components, low-loss operation requires careful design of not only individual waveguide components, but also the transitions between different waveguide geometries and integration platforms.

In this contribution we will present our recent work on design and characterization of passive optical components including splitters, filters, polarization handling components and fiber couplers in different material platforms. Particular emphasis will be placed on optical interfaces, which often represent a major limitation in practical photonic systems. Optical losses arising from fiber-to-chip and chip-to-chip interfaces are frequently among the primary factors limiting the overall efficiency, scalability, and applicability of PIC-based systems.

Photonic wire bonding (PWB) has recently emerged as a promising technology for efficient, reliable and scalable optical interconnects between optical fibers and PICs. PWB uses two photon lithography to form free-standing polymer waveguides that can bridge separate optical components with high flexibility and relaxed alignment tolerances. Sub-dB losses have already been demonstrated for various kinds of PWB interfaces, however, in many cases there remains significant room for further improvement. In particular, the transition from the on-chip waveguide to the free-form PWB waveguide, typically implemented by a surface taper structure can represent a dominant contribution to the overall insertion loss of the PWB interface.

We will present a novel design strategy for improving this transition by introducing a short multi-mode bend section in the PWB waveguide. The proposed approach reduces substrate leakage at the chip-to-polymer interface and enables more efficient air-clad PWB coupling without relying on additional polymer overcladding.

Robust Coupler Design for Efficient Heterogeneous Integration of Quantum Photonic Devices

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Photonic integrated circuits are important for the advancement of optical communications, sensing and imaging technologies, neuromorphic computing, and quantum technologies. A key trend in this field is the heterogeneous integration of devices based on distinct material and fabrication platforms in a single chip [1]. This is especially important for quantum photonic integrated circuits (QPICs), because it enables the co-integration of the best classical and quantum photonic components—such as single-photon sources, detectors, modulators, and ultra-low loss routing structures [2]. This is absolutely critical to satisfy the stringent low-loss performance requirements of quantum applications.

Techniques like micro-transfer printing (μ TP) enable the physical integration of diverse components. However, to ensure reliable low-loss operation, the optical interfaces in between them must be carefully designed with real-world operating conditions in mind [3]. In our contribution, we will present a novel approach to the design of optical couplers focusing on high coupling efficiency robust against critical fabrication-induced structure variations. In particular, we will show the design of adiabatic mode couplers between a GaAs platform hosting state-of-the-art single-photon sources based on InAs quantum dots and an ultra-low loss silicon nitride (SiN) interposer platform, heterogeneously integrated through μ TP. Here, we consider the effects of μ TP-induced misalignment and other geometrical deviations of the structure, as well as propagation losses caused by sidewall roughness of GaAs waveguides—a critical optical loss mechanism. We will show both simulation results and preliminary experimental results from fabricated devices.

Acknowledgements

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Design of a Photonic Master for Nanoimprint Lithography of Perovskite Layer in Integrated Photonic Circuits

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Metal halide perovskites have emerged as promising materials for integrated photonics due to their excellent optical properties, solution processability, and compatibility with scalable fabrication techniques. However, efficient optical coupling and precise photonic structuring remain significant challenges for perovskite-based photonic integrated circuits (PICs).

In this work, we present the design of a tailor-made silicon nitride (SiN) photonic master chip for replication of photonic integrated components into CsPbBr_3 perovskite layer by means of nano-imprint lithography (NIL). The components on the master were designed considering the refractive index of the fabricated perovskite layer on glass substrate.

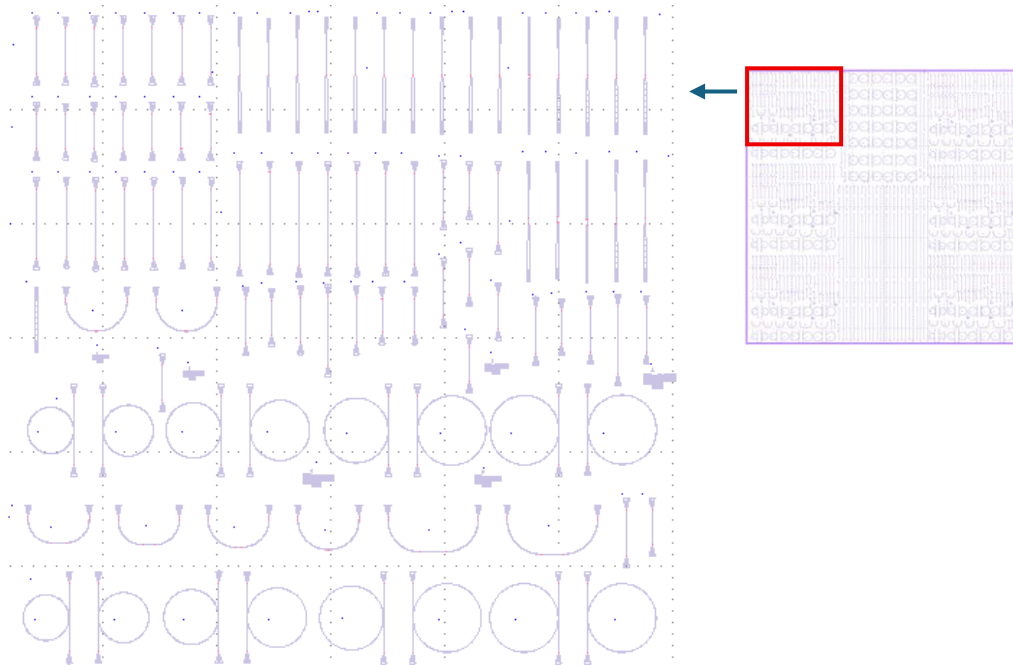


Figure 1: Layout of the tailor-made SiN photonic chip designed as a master template for CsPbBr_3 perovskite pattern transfer. The highlighted section represents the main unit cell, which is replicated across the chip to evaluate pattern transfer fidelity and reproducibility.

The work focuses on the simulation-driven design and optimization of photonic building blocks for testing efficient light coupling and propagation losses in embossed perovskite based (passive) PIC. Multiple grating coupler architectures, including focused grating couplers and rectangular grating couplers, were designed and numerically investigated to evaluate their coupling performance. Key grating parameters such as pitch, fill factor (FF), etch depth, and grating geometry were systematically varied to identify optimal coupling conditions. In parallel, different waveguide widths were studied, including 800 nm, 900 nm, and 1000 nm, to determine the most suitable dimensions for single-mode propagation and efficient mode overlap with the grating structures.

Beyond coupling structures, additional passive photonic components were incorporated into the chip design to evaluate integrated photonic functionality. These included ring resonators, racetrack resonators, and loopback structures, designed with varying radii to study propagation behavior, bending effects, and transmission characteristics. Loopback configurations were included to enable direct estimation of coupling and propagation losses, providing a practical platform for future optical characterization. The optimized SiN chip for optical guiding in final perovskite chip serves as a high-resolution reusable master for subsequent Nanoimprint lithographic replication. SiN PIC was used as a master for the reason of comparable refractive indices with perovskite layer. In such a way, photonic structures can be partially tested on the master before replication on perovskite film. In the NIL process a polydimethylsiloxane (PDMS) replica was fabricated from the SiN master chip and used to transfer nanoscale photonic patterns into CsPbBr₃ films deposited on a cleaned glass substrate. This strategy combines the precision of silicon nitride nanophotonic design with the scalability and low-cost processing advantages of perovskite-compatible soft lithography. This work establishes a simulation-guided framework for the development of perovskite-compatible photonic platforms and provides the design foundation for future realization of patterned CsPbBr₃ integrated optical devices.

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Design of Silicon Nitride Integrated Photonic Components for In-House Photonic Platform Characterization

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Photonic integrated circuits (PICs) are chips that combine many photonic components on a single substrate similarly as electronic integrated circuits combine multiple electronic components. PICs transmit, manipulate and detect light signals (photons) instead of the electrical signals (electrons and holes). PICs are used in various applications including optical communications, sensorics, quantum applications, computing and metrology systems [1]. For different applications, different photonic platforms have been established including silicon on insulator, silicon nitride (SiN), III-V semiconductors, lithium niobate, thin film lithium niobate and tantalate, polymers and others [2]. The most established platforms due to their compatibility with CMOS fabrication process are silicon on insulator and silicon nitride platforms. Silicon nitride (SiN) platform is used in applications where wide optical transparency window from visible to mid-infrared light and low loss is required since the SiN material inherently exhibits these properties [3]. Passive components of PIC are light guiding components (waveguides), power splitters (multi-mode interferometers (MMI), directional couplers), resonators (ring-resonators, Bragg gratings) and interferometers (Mach-Zehnder interferometer).

The fabrication process of PIC platforms majorly affects the quality of the platform, especially the minimal feature size and minimal spacing, which in turn determine critical dimensions and performance of integrated components and devices. For a new fabrication process, these parameters need to be determined since as stated they are crucial for device design and optimization. Based on the determined parameters, devices for characterization of the new fabrication platform can be designed, which provide insight into the platform characteristics such as scattering and bend loss, optical bandwidth and device repeatability across the fabricated PIC and whole wafer.

In our contribution we will present design process of selected basic photonic components and PIC for characterization of current in-house SiN photonic platform based on sub-micrometer CMOS technology. In this design we want to test optical losses for different wavelengths and possible current state technology use for different applications, such as sensorics. Based on previous experiments we will focus on the characterization of minimal dimensions and spacing, where we will determine minimal usable dimensions of waveguides and power splitters for different wavelengths including 1550 nm, 930 nm and 630 nm, which are used in different photonic applications such as optical communication, quantum applications, metrology and sensor applications.

During the design process we will first consider the measurements of minimal feature sizes of fabricated structures and spacings based on the PIC already fabricated on this fabrication platform. The measurements were determined from the scanning electron microscope images of fabricated waveguides and waveguide structures. We will design and optimize the waveguides for all wavelengths with waveguide mode analysis, using finite difference eigenmode simulations which will determine the optimal width of the waveguides. For characterization of optical losses on the platform, we will design waveguide spirals and ring resonators. Due to minimal spacing requirements, we will design 1x2 and 2x2 MMI with splitting ratios of 50%/50% and 85%/15% straight to cross

splitting ratios. We will begin designing the MMIs with the analytical approach and based on the dimensions calculated analytically we will perform numerical optimization with finite difference time domain numerical simulations. From the designed MMIs, we will construct multiple all-pass and add-drop ring resonators with different combinations of MMIs and multiple bend radiuses and ring lengths with which we will aim to get either critical coupling or deep resonances which will be used after the fabrication to determine the loss in the waveguides. We will design cutback structures for characterization of MMIs and multiple sets of waveguide spirals for scattering and bend loss characterization. Dedicated passive structures, such as ring resonators and MZI structures, which will be designed for possible use in sensoric applications in combination with microfluidics.

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Design of Fabrication-Tolerant Multimode Interference Splitters in Silicon Nitride Photonic Integrated Circuits

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Abstract:

Among various optical splitter structures in photonic integrated circuits, multimode interference (MMI) splitters can achieve target splitting ratios and low losses, largely independently of device size. Since this can be controlled by appropriately choosing the dimensions of the MMI, larger structures with stable splitting ratios and lower losses can be fabricated while remaining more tolerant to fabrication imperfections, making them especially attractive for fabrication processes with limited resolution. In this paper we present a numerical study of fabrication tolerance in MMI splitters for various splitting ratios and operating wavelengths. We also present a tolerance study of MMI structures with arbitrary splitting ratios. Numerical solvers such as Eigenmode Expansion (EME) and Finite-Difference Time-Domain (FDTD) methods are used for light propagation simulations. Based on the results, the relationship between the geometrical properties and the structure's tolerance is established. Optimal designs are obtained that provide deviations in transmission as small as 1% in the case of a 0.1 μm lithography fabrication error and 1 μm spatial resolution, for various splitting ratios. The results also show sufficient tolerance of splitters with arbitrary ratios, such that they could be used in high-quality-factor resonators. Based on these findings, we establish a comprehensive set of robust, fabrication-tolerant optical splitters for use in photonic integrated circuits (PICs).

Keywords: Photonic integrated circuits; Multimode interference; Fabrication tolerance;

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1 Introduction

In recent years, silicon photonics has gained significant attention with applications ranging from telecommunications, optical computing and sensing to quantum technologies, particularly because of its CMOS compatibility. Among CMOS-compatible material platforms, silicon nitride stands out due to its broad transparency window and ultra-low propagation losses, which are especially important for quantum applications [1]. The performance of many PIC components strongly depends on fabrication quality, and reliable performance often requires state-of-the-art high resolution fabrication processes. Optical splitters such as directional couplers (DCs) and multimode interference (MMI) splitters, which are key components of filter and resonator structures, are particularly susceptible to splitting-ratio deviations and increased losses caused by fabrication imperfections. Figure (1a) shows typical MMI splitter with geometrical parameters, that will be discussed later. Figure (1b) shows typical DC structure with the gap width W_{gap} .

For DCs, one way to mitigate these effects is to increase the gap between the coupled waveguides, making fabrication deviations relatively smaller. However, this comes at the cost of substantially longer device lengths. Compared to DCs, MMI splitters can achieve target splitting ratios and low losses, largely independently of device size. By exciting multiple modes within the multimode section and positioning the outputs at locations where so-called self-images appear, low loss power splitting may be achieved [2], [3]. Since this can be controlled by appropriately choosing the dimensions of the MMI, larger structures with stable splitting ratios and lower losses can be fabricated while remaining more tolerant to fabrication imperfections, making them especially attractive for fabrication processes with limited resolution.

While MMIs offer these tolerance advantages, their design flexibility in terms of achievable splitting ratios remains limited, due to constraints inherent to the self-imaging process. This is particularly limiting for applications such as ring resonators and other filtering structures, which require weak and precisely controlled coupling strengths to achieve a high-quality factor [4]. The need for fabrication-tolerant arbitrary ratio splitters is therefore evident.

In this work, we address this need in two steps. First, we analyze how the geometrical parameters of an MMI affect its fabrication tolerance. Second, we introduce a design method for achieving arbitrary splitting ratios while preserving this fabrication tolerance.

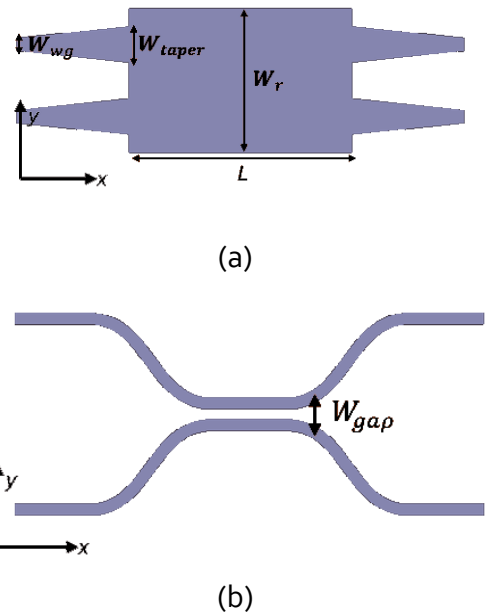


Figure 1: (a) typical 2x2 MMI with output ratio:50/50. (b) typical 2x2 DC with the same ratio. Blue represents SiN layer on SiO₂ substrate.

2 Methods

In our work we utilized numerical simulations to design and analyze MMIs.

We used the Ansys Lumerical package for light propagation simulations. First, the Eigenmode (MODE) solver was used to calculate the effective index of the propagating mode inside the waveguides [5]. This effective index is used to determine the input waveguide geometry and the splitting ratio in arbitrary-ratio MMIs.

For transmission calculations and to determine the self-imaging length in regular MMI structures we used the Eigenmode Expansion (EME) solver, since it offers a significant speed advantage over the Finite-Difference Time-Domain (FDTD) solver [6]. The accuracy of the EME method was verified by comparing its results with FDTD simulations.

Since accurate phase accumulation is key to achieving reliable results for arbitrary ratio MMI splitters [7] and since the EME method lacks the required resolution, only FDTD simulations were used in that case.

3 MMI design

3.1 Theoretical background

When a TE or TM mode propagating in a single-mode access waveguide enters a much wider multimode section, it excites a set of higher-order modes. These modes interfere constructively at specific propagation distances, reproducing so-called self-images of the input field [8]. By positioning the output waveguides at these lengths, a precise splitting ratio can be achieved.

$$L = \frac{p}{2}(3L_\pi), \text{ where } L_\pi \cong \frac{n_r W_e^2}{3\lambda_0}, p = 1, 3, 5 \quad (1)$$

$$\Delta L \cong \frac{p \cdot n_r W_e}{\lambda_0} \cdot \Delta W_e \quad (2)$$

In eq. (1), which is analytically derived from modal propagation analysis [8], L_π is defined

as the beat length of the two lowest order modes and is quadratically dependent on the width of the field, which is almost equal to the width of the multimode section W_r ; n_r is the effective index of the fundamental mode propagating in multimode waveguide, λ_0 is the operating wavelength and L is the length of the core, where two self-images of the input mode appear, providing a precise splitting ratio. If the actual physical length of the multimode section deviates from the self-imaging length, the device exhibits high excess loss and an imbalanced splitting ratio. We used a fabrication error of $0.1 \mu\text{m}$ in the x and y axes as our benchmark value, representing a relatively high-error fabrication process.

As shown in eq. (2), the shift in self-imaging length is inversely proportional to the operating wavelength, therefore the structure becomes less tolerant to fabrication errors at shorter wavelengths.

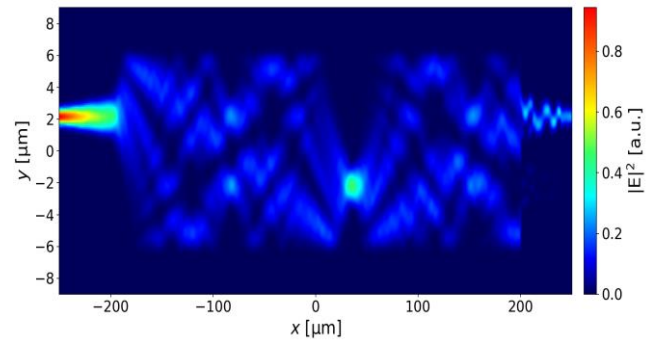


Figure 2: Field intensity profile of light propagation inside MMI. Multiple self-images appear at different positions in x direction.

Table 1: Self-imaging lengths and their splitting ratio.

Length	Splitting ratio
$\frac{1}{2}(3L_\pi)$	50 / 50
$3L_\pi$	100 / 0
$\frac{3}{2}(3L_\pi)$	50 / 50

Figure (2) shows electric field profile inside the MMI, several self-images appear at lengths, which are listed in Table (1) with their

corresponding splitting ratios. A precise ratio may be chosen from a set of configurations by adjusting the positions of the input and output waveguides [9].

The multimode section has a significantly larger width than an input waveguide, which causes a large discontinuity in effective refractive index n_{eff} of the propagating mode between the input section and the multimode section. Changes in n_{eff} produce high reflectivity at this boundary. Therefore, tapered waveguides with width W_{taper} , which slowly increase n_{eff} , are used to minimize back reflection.

3.2 Arbitrary ratio splitters

Arbitrary-ratio MMIs in various topologies have been broadly investigated in the literature [10]. We decided to proceed with so-called angled MMIs, since these structures can be fabricated with low resolution processes [11],[12]. Such MMIs require a $3L_\pi$ length of the multimode section in the 50/50 configuration, so that 50/50 self-images appear at the center of the section, and another 100/0 self-image appears at the output, as seen in Figure (3). By bending the multimode section to create a path difference between the 50/50 constructive interferences, we induce a phase shift that depends on the bend angle. The propagating modes then interfere at the output section like two coherent waves, one of which carries an additional phase. The final splitting ratio therefore depends on the bend angle, and a 100/0 splitting ratio is transformed into an angle-dependent splitting ratio, described by eq (3) [11].

$$T = \cos^2(\varphi) \quad (3)$$

$$\varphi = \tan \theta \cdot 2S \cdot k_0 \quad (4)$$

T is a light intensity in output cross waveguide, where φ is the phase induced by bending the multimode section by an angle θ . S is a position of the input waveguides equal to $\frac{W_r}{3}$

for 50/50 configuration and k_0 is the propagation constant of the fundamental mode inside the multimode section.

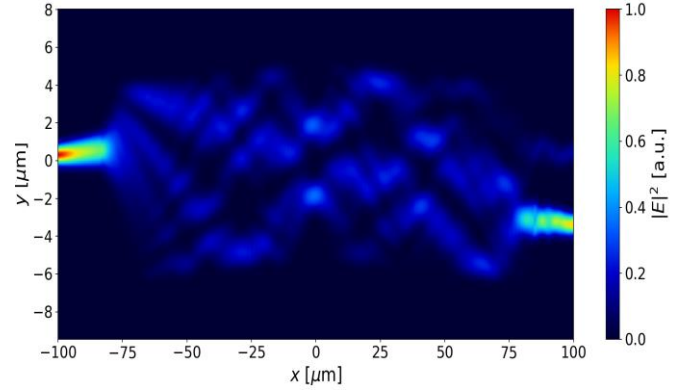


Figure (3) Field intensity profile of light propagation inside an angled MMI. 50/50 self-images appear at the center of multimode section, where phase shift occurs. 100/0 output ratio transforms into 85/15, with maximum at the cross output.

4 Results

4.1 Precise ratio splitters

Previous tolerance study for 1×2 MMIs revealed that increasing the width W_{taper} of the input and output tapers enhances the structure's tolerance to deviations in length and width; however, increasing W_{taper} also decreases the output transmission [13].

We proceeded to further investigate 2×2 MMI and arbitrary ratio MMI. The study was conducted for 50/50, 85/15 and 15/85 splitting ratios. To achieve 50/50 ratio, waveguides were positioned at $\frac{W_r}{3}$ and $\frac{2W_r}{3}$ [9]. For 85/15 the positions were $\frac{W_r}{4}$ and $\frac{3W_r}{4}$ [9]; therefore, the maximum width of the taper was greater in the 85/15 configuration. To achieve 15/85 splitting ratio, as seen from Figure (2), the length needed to be increased 3 times since self-image reappears in a flipped version.

Since the length increases quadratically with W_r , we constrained ourselves to 13 μm multi-

mode section width for all three splitting ratios. The optimal length for each device was calculated with the EME solver by sweeping the length of the multimode section. In Figure (4) the transmission at the cross and bar outputs is shown in dependence of the core length.

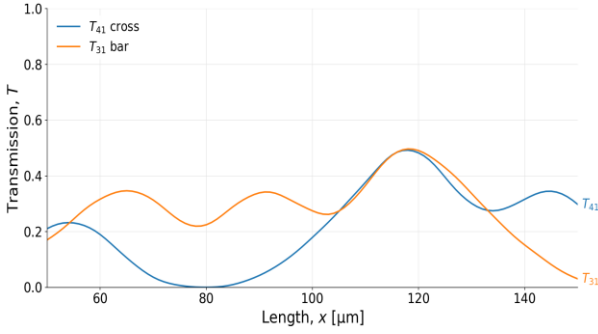


Figure 4: Transmission vs L at output monitors, x-axis being L , y-axis being T with both peaks of 0.5 transmission being at the same length.

We then proceeded with obtaining a correlation between taper width and fabrication tolerance. Figure (5a) shows the transmission color plot for 50/50 configuration depending on taper width and fabrication error; Figure (5b) shows the same relationship for 85/15 configuration. At larger W_{taper} , a structure becomes more tolerant. For our case of 1 μm minimal feature size, we had a clear constraint on the maximum available width. Since the main goal was to optimize the design for the best achievable tolerance we proceeded with the maximum available width. Figure (6) shows the fabrication error tolerance of both configurations at the maximum taper widths allowed by the minimal feature size. Figure (6a) shows the transmissions in dependence of multimode section width fabrication error. Figure (6b) shows the transmissions normalized to their peak values. Since a larger taper width can be achieved in the 85/15 configuration than in the 50/50 configuration, the 85/15 configuration exhibits a higher tolerance. Therefore, to achieve the same tolerance, the multimode section width for the 50/50 configuration needs to be greater, resulting in a

larger overall structure. Since the 15/85 splitting ratio requires a three-times-longer length, deviations in width further displace the self-image from its designed position; we can therefore anticipate a higher transmission deviation. This can also be observed in Figure (6b).

Transmission of the 85/15 cross output at an operating wavelength of 930 nm is also shown, confirming the reduced tolerance to fabrication errors at shorter wavelengths, as described in the theoretical background (Section 3.1).

Presented designs achieve a 1% deviation for precise-ratio MMIs in the worst-case fabrication error, which allows us to establish a robust set of splitters for low-resolution fabrication processes.

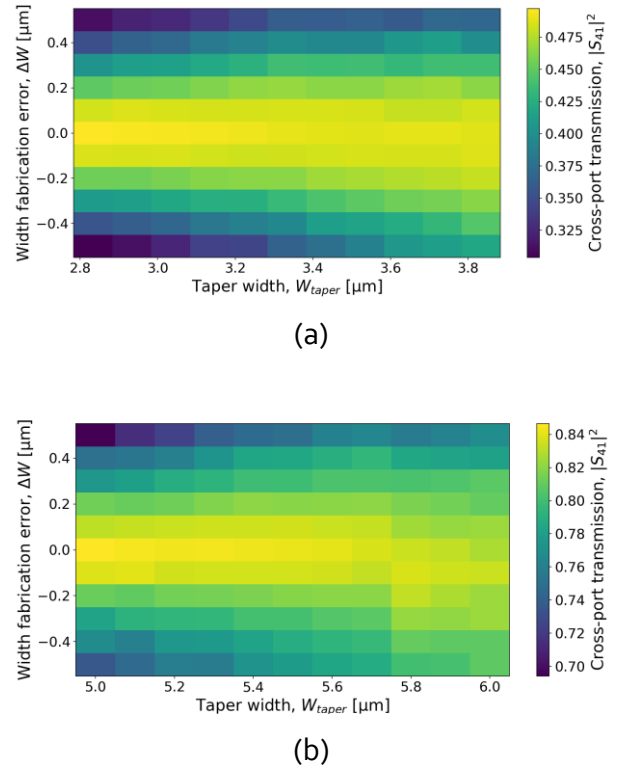
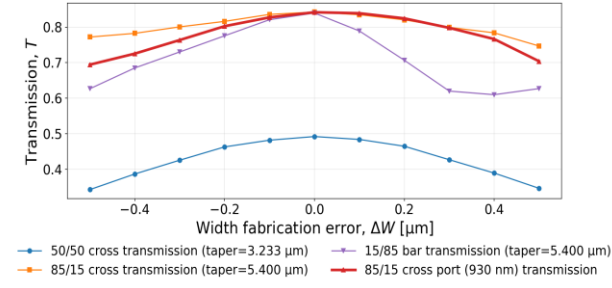
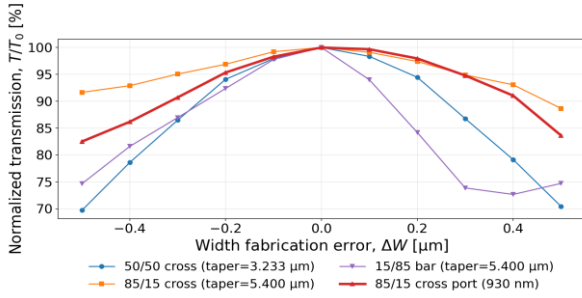


Figure 5: Cross port transmission vs. W_{taper} on x axis and fabrication error on y-axis for a 50/50 configuration (a) and 85/15 configuration (b).



(a)

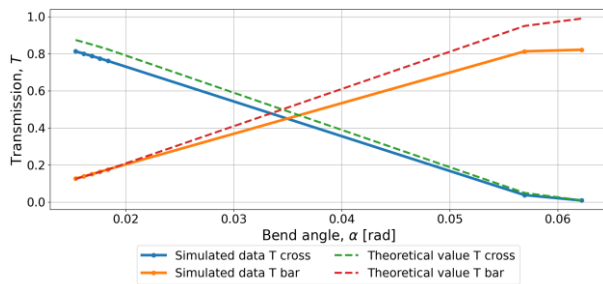


(b)

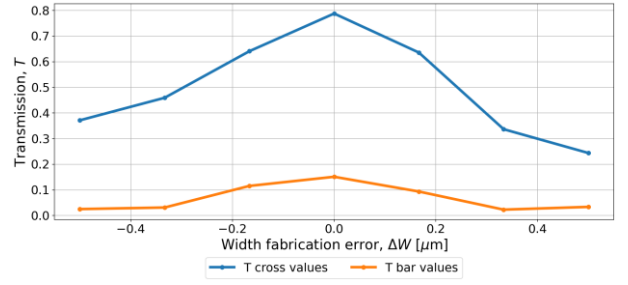
Figure 6: Comparison of 50/50 and 85/15 (15/85) configurations a) absolute values b) normalized transmission to the peak value.

4.2 Arbitrary splitting ratio tolerance study

We used the 50/50 configuration and first obtained the optimal length L of the MMI using the EME method. The multimode section length was then doubled to achieve a 100/0 ratio at the output. We performed an angle sweep, followed by a W_r sweep at a multimode section length equal to $2L$. Since a deviation in width shifts the position of the 50/50 self-image away from the bend, these structures are considerably more unstable than precise-ratio structures.



(a)



(b)

Figure 7: (a) Transmission of both output ports vs angle of bend. Dashed lines represent squared cosine values of simulated angles. (b) Transmission vs fabrication error.

Figure 7(a) shows the transmission of the angled MMI as a function of bend angle, with dashed lines showing the calculated values from eq. 3 for comparison. We simulated densely around the angles corresponding to an 85/15 ratio and simulated two additional angles corresponding to the 10/90 and 5/95 ratios. As seen in the figure, the structure exhibits high loss at larger angles. Figure 7(b) shows the structure's response to fabrication deviation: at a $0.1 \mu\text{m}$ fabrication error, the transmission falls by 10%. However, it should be noted that these simulations were performed with W_r equal to $11 \mu\text{m}$ to reduce computation costs.

Still for arbitrary ratio applications MMI splitters exhibit excellent fabrication error tolerance compared to their DC equivalent with similar dimensions. A stable coupler is required to achieve stable resonator and filter structures. Another possible application of such structures is in higher-quality processes, since the coupling properties of MMI may vary less across the wafer as well [14].

5 Conclusion

A tolerance study was conducted for precise-ratio 2×2 MMIs, as well as for arbitrary-ratio MMIs in an angled topology. The relationship

between geometrical properties and fabrication tolerance was established for both structure types. For precise-ratio splitters, optimal designs were shown to achieve deviations in transmission as small as 1% under a worst-case 0.1 μm lithography error and 1 μm spatial resolution, with wider tapers and larger multimode section dimensions improving tolerance. For arbitrary-ratio splitters, the proposed angled MMI method was shown to provide angle-dependent splitting ratios with sufficient tolerance to fabrication imperfections, substantially exceeding that of directional couplers of comparable size, although at a higher computational cost during design. The high loss at larger angles could potentially be solved by creating a buffer section between the two cuts, as described in [12], and requires further investigation.

6 Acknowledgements

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OPTOELECTRONICS

Interplay of Corrugation Geometry and Dipole Orientation on Light Extraction in Organic and Perovskite LEDs

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Abstract: Perovskite (PeLEDs) and organic (OLEDs) light-emitting diodes share a thin-film microcavity architecture and dipole-based emission mechanism, resulting in similar light-outcoupling limitations in conventional planar devices. The main optical losses originate from total internal reflection due to refractive-index mismatches and from absorption at metallic electrodes through coupling to surface plasmon polaritons (SPPs). Consequently, many light-extraction concepts developed for OLEDs are potentially transferable to PeLEDs. In this work, we introduce internal nano-corrugations into a blue OLED device and examine their combined effect with emitter dipole orientation on light extraction using a three-dimensional finite-element method (FEM) optical model employing a Floquet approach. The model is first validated against a benchmark optical model and an extensive simulation dataset. Our results identify the corrugation aspect ratio ($AR = \text{height/period}$) as the critical design parameter, with an optimum value of approximately 0.3 for isotropic dipole distributions. Light-extraction enhancements of up to 20% relative to planar devices are achieved over a broad corrugation-period range of 600-1000 nm. The efficiency improvement is primarily attributed to corrugation-induced suppression of SPP losses, complemented by waveguide-mode extraction and increased light scattering. These findings establish practical design guidelines for enhancing light outcoupling in OLEDs and next-generation PeLEDs.

Keywords: OLED; PeLED; finite element method; corrugations; anisotropy

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1 Introduction

Organic light-emitting diodes (OLEDs) are a key technology for modern displays and solid-state lighting due to their high contrast, excellent colour quality, wide viewing angles, and compatibility with large-area fabrication. More recently, perovskite light-emitting diodes (PeLEDs) have emerged as a promising complementary technology, offering narrow emission spectra, tunable wavelengths, high photoluminescence quantum yields, and rapidly improving efficiencies. Both technologies

combine low manufacturing costs, high energy efficiency, and compatibility with thin, lightweight, flexible, and transparent substrates, making them attractive for next-generation optoelectronic applications [1], [2], [3].

OLEDs achieve near-unity internal quantum efficiency through phosphorescent emitters and thermally activated delayed fluorescence (TADF) materials [4], [5]. Likewise, state-of-the-art PeLEDs exhibit near-unity radiative efficiencies owing to the outstanding optoelectronic properties of metal-halide perovskites

[6]. However, the external quantum efficiency (EQE) of conventional planar devices is typically limited to 20–30%, as a significant fraction of generated photons remains trapped within the device due to optical losses [7].

These losses mainly arise from three mechanisms: substrate modes caused by total internal reflection (TIR) at the substrate-air interface, waveguide modes confining light to the device thin layers, and coupling to surface plasmon polaritons (SPPs) at metal interfaces. Additional losses come from parasitic absorption, making light extraction an important challenge for both OLEDs and PeLEDs.

Among the many proposed outcoupling strategies [8], [9], surface corrugation and preferential emitter dipole orientation have proven particularly effective. In this work, we investigate their combined effect on light extraction. We consider two-dimensional sinusoidal substrate textures with periods of 450–1500 nm and varying heights, coupled with a layer-growth model that accounts for isotropic and conformal deposition processes [10]. This approach captures the evolution of realistic device morphologies and non-uniform layer thicknesses.

Our results show that sinusoidal corrugations strongly enhance light extraction for vertically oriented dipoles, primarily by reducing coupling to SPP modes. In contrast, horizontally oriented dipoles benefit only marginally and may even exhibit lower extraction efficiencies than planar devices for certain texture dimensions. While a broader parametric study is presented elsewhere [11], this work focuses mainly on the modelling approach.

2 Modeling

Optical simulations were performed using two optical models for flat and corrugated devices, based on transfer matrix method (TMM) and finite element method (FEM) methods, respectively. Both models are used to evaluate

the light outcoupling and extraction efficiencies, defined as the ratio of the light generated in the emissive layer (EML) to the light extracted into air or into the substrate, respectively. Because the models have been comprehensively described elsewhere [12], [13], only a brief summary of their underlying mechanisms is given here.

The first model, for optically thin layer stack, consists of TMM method, where instead of external sources, we modified it to contain internal sources, with plane waves representing emission sources, considering different orientation and polarization. The TMM is then combined with ray tracing for the optically thick (micro-textured) substrate, with back reflected rays being again used with non-modified TMM. The combined model was verified experimentally to adequately represent real working devices [12], [14], [15].

Second model is based on a standard 3D finite element method (FEM), and is constructed in a commercial software Comsol [16]. This model enables us to simulate nano-textured OLEDs and PeLEDs with a single incoherent dipole source in an otherwise periodic structure [17], [18]. We limit the simulations to a single unit cell, containing a single period in each lateral direction. Semi-infinite domains (glass substrate, air) are truncated with absorbing (scattering) boundaries with negligible reflectivity. On the periodic sides of the unit cell, we apply Floquet periodic boundaries, a pair in each direction, where by employing multiple Bloch terms we successfully eliminate emission source coherence effects. Using this approach we highly reduce computation costs, compared to sufficiently large model. On the other hand, a sufficient number of Bloch terms need to be simulated, to successfully eliminate coherence effects, increasing simulation time. Although, more simulations need to be done with Floquet method, a much lower requirements on computational resources and possibility of parallel computing outperform simulations on large models.

Moreover, the process itself requires some special care, when constructing the model, especially for periodic faces where identical (node-to-node) meshes need to be used, as well as the open boundaries need to be sufficiently far away (at least λ) from thin-film stack. The meshing needs at least 5-6 elements per effective wavelength and quadratic (second-order) vector elements for electric field. Further details in papers [11], [13].

In both models emission sources can be simulated as differently oriented point dipoles located within the thin-film structure. These dipoles are generally considered to possess an isotropic in-plane distribution while potentially exhibiting a preferential distribution relative to the normal of the layer stack. This preferential distribution can be described by the anisotropy factor α , defined as the ratio of vertically oriented dipoles to all dipoles. The factor simplifies complex dipole-orientation distributions to a ratio of parallel and perpendicular dipole moments. Thus, $\alpha = 0$ represents the ideal horizontal orientation of all dipoles, whereas $\alpha = 1/3$ represents an isotropic orientation with the equal ratio of vertical and horizontal dipoles.

3 Results

Despite possible differences between OLEDs and PeLEDs in several important aspects, including emission-layer thickness, emission distribution, refractive index, photon recycling, and film morphology, they share many fundamental optical characteristics. Therefore, the results presented here are relevant to both technologies, provided that their specific material and device differences are taken into account.

3.1 Simulated structures

Here, we present a limited set of representative results obtained for blue OLEDs only. However, the proposed methodology and the

underlying physical insights are equally applicable to devices emitting at other wavelengths [13] as well as to related PeLED technologies. The investigated device architecture is based on a conventional blue OLED stack [19], consisting of an emissive layer (EML) sandwiched between an electron transport layer (ETL) and a hole transport layer (HTL). Charge injection is provided by an opaque silver cathode and a transparent indium tin oxide (ITO) anode. The complete thin-film structure is assumed to be deposited on either a planar or a textured glass substrate – Figure 1.

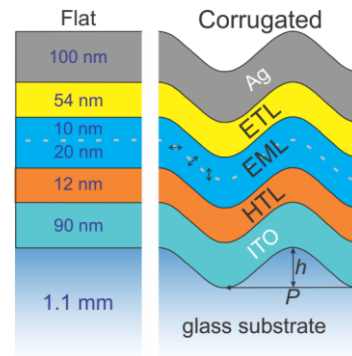


Figure 1: Simulated device schematics on flat and corrugated substrates in a 2D cross-sectional view. Functional layers are labeled together with their respective thicknesses, and the corrugation period (P) and height (h) are indicated.

Each layer of the device is characterized by its thickness and corresponding complex refractive index. For nanostructured devices, the surface texture is explicitly incorporated into the model, together with the resulting conformal layer growth during device fabrication [10]. The emission sources are positioned at a specific vertical location within the EML, reflecting the non-uniform carrier distribution typically observed in OLEDs.

3.2 Optical model validation

Prior showing the main results, we want to show the validation of the proposed model, which is based on methodologies previously

reported in the literature [17], [18]. The modelling framework has been extensively validated for planar OLED structures, for which both experimental measurements and exact transfer-matrix calculations are available [12], [14], [20]. In these studies, the model accurately reproduced light-outcoupling characteristics across a broad range of planar device configurations.

While the model has been thoroughly validated for planar structures, extension to nano-textured devices requires additional verification because corrugated geometries exhibit fundamentally different optical behaviour. The accuracy of the method was assessed through comparisons with alternative numerical modelling approaches.

The investigated system consists of a single emitting dipole embedded within an otherwise infinitely periodic structure. A direct numerical treatment of such a configuration can be achieved by simulating a laterally extended domain with appropriate absorbing boundary conditions, thereby approximating the response of an infinite periodic environment. Although this approach is feasible in two-dimensional simulations, the computational requirements become prohibitive for large three-dimensional domains. Consequently, the primary validation was performed by comparing results obtained using the Floquet-based formulation on a 2D modelling approach.

For the two-dimensional case, a one-dimensional sinusoidal texture with a period of $P = 800$ nm and a height of $h = 240$ nm was considered. Simulations were performed for five distinct dipole positions, with horizontal and vertical dipole orientations treated separately – Figure 2(a). The reference calculations employed a computational domain comprising 19 unit cells, whereas the Floquet-based approach utilized a single unit cell. The comparison, presented in Figure 2(b,c), shows excellent agreement between the two methods for all dipole positions (see Figure 2(a) for position

location) and orientations, thereby supporting the validity of the Floquet formulation for periodic textured structures.

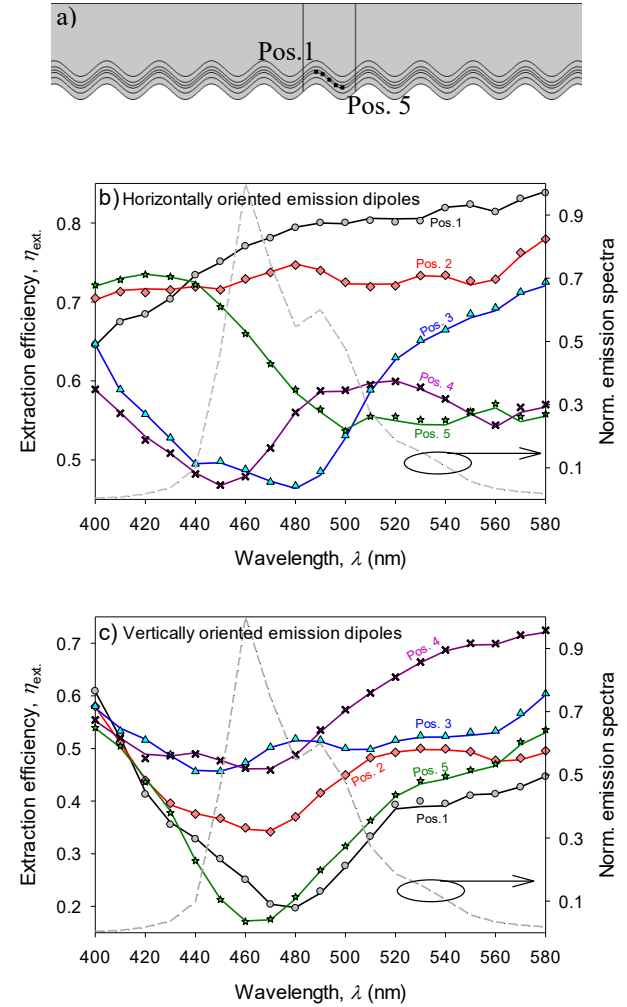


Figure 2: a) Schematics of a “large” 2D model. b,c) Simulated extraction efficiency for large (lines) and Floquet (symbols) model. b) horizontal -, c) vertical- orientation of emission dipoles.

Although two-dimensional simulations provide a computationally efficient platform for method verification, they cannot fully represent the physical behaviour of emitting dipoles, which are inherently three-dimensional sources. Therefore, additional validation was carried out using full three-dimensional simulations. Due to the substantially increased computational cost, a single representative case was investigated, corresponding to a blue OLED with period ($P = 800$ nm), height ($h =$

240 nm) and at single emission (peak) wavelength ($\lambda = 460$ nm). The analysis included 15 distinct dipole positions and considered two orthogonal horizontal dipole orientations together with a vertical orientation.

The three-dimensional reference model consisted of a 5×5 array of unit cells – Figure 3(a), while the Floquet-based simulation again employed a single unit cell. Figure 3(b) compares the resulting light-extraction efficiencies obtained with both approaches. A good agreement between the large-domain and Floquet-based simulations is observed, providing further evidence of the validity of the proposed methodology in three dimensions. The level of agreement is slightly lower than that obtained in the two-dimensional analysis, which is attributed to the smaller computational domain used in the reference three-dimensional model as a consequence of the available computational resources.

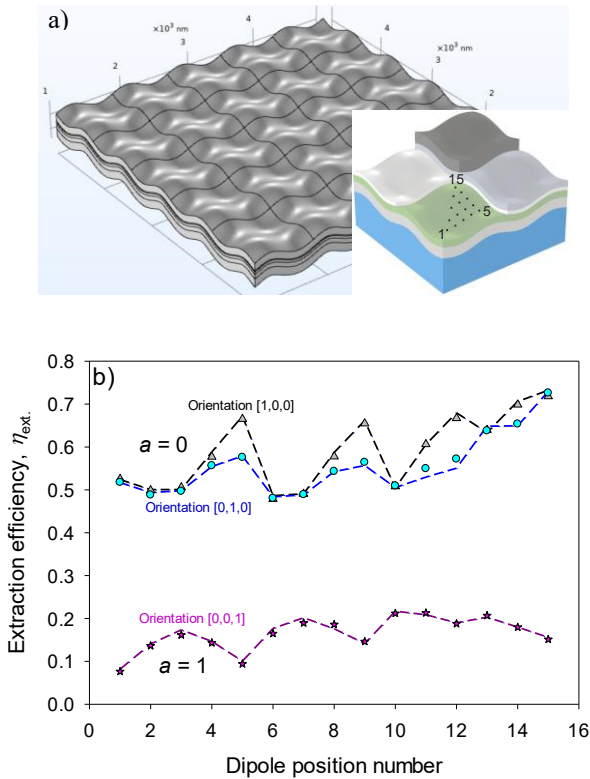


Figure 3: a) Schematics of a “large” 3D model b) Simulated light extraction for large (lines) and Floquet (symbols) model for 15 dipole positions (see inset) and 3 basic orientations.

This comparison demonstrates that the Floquet-based approach accurately reproduces the results of significantly larger computational models while requiring only a fraction of the computational resources, making it well suited for the analysis and optimization of periodically textured OLED structures.

3.3 Light extraction in blue OLEDs

To investigate the influence of corrugation geometry on light extraction, simulations were performed for 2D sinusoidally textured devices with varying texture P and h - Figure 4.

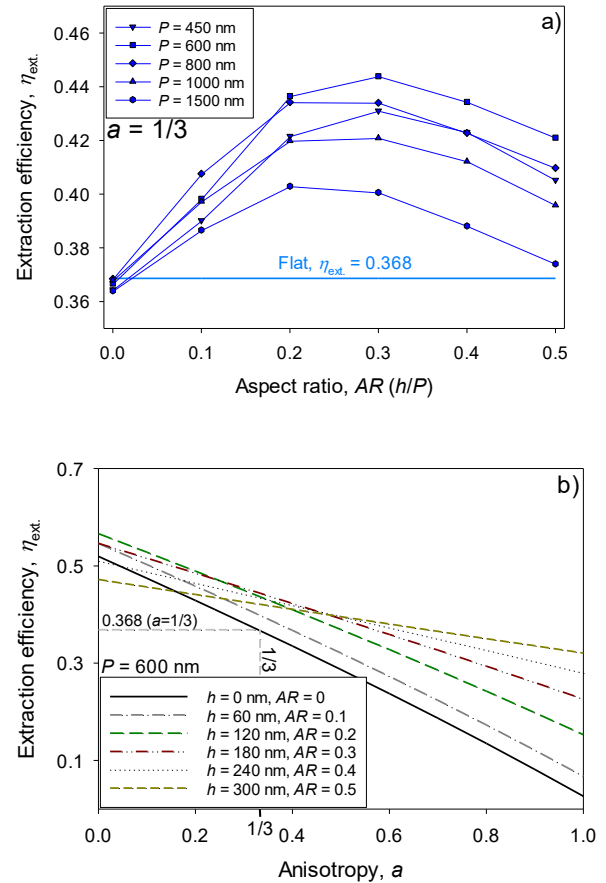


Figure 4: a) Extraction efficiency (in glass substrate) in dependence of AR for different P and $a = 1/3$. Small differences at $AR = 0$, are due to numerical mistakes due to coarser mesh settings for large P . b) Light extraction regarding to initial anisotropy for corrugation of $P = 600$ nm and different ARs.

Light extraction was evaluated separately for horizontally oriented (x , y) and vertically oriented emission dipoles, as well as for an isotropic dipole ensemble ($a = 1/3$). Treating horizontal and vertical dipoles independently establishes a basis for evaluating arbitrary preferential dipole orientations in subsequent analyses.

We show here data for $a = 1/3$, where for all considered texture aspect ratio ($AR = h/P$), the overall behaviour was found to be largely independent of the actual texture P . For an isotropic dipole distribution ($a = 1/3$), the highest overall light extraction is obtained for $AR \approx 0.3$, regardless of the actual texture P , with highest extraction observed for $P = 600$ nm with up to 20% improvement in light extraction – Figure 4(a).

Assuming that the dipole distribution remains unchanged across the textured surface, the dependence of light extraction on the general dipole orientation was further evaluated. The corresponding results for a texture period of $P = 600$ nm and several corrugation heights are shown in Figure 4(b). In this analysis, the dipole orientation is fixed with respect to the global coordinate system and does not locally follow the surface profile. The results demonstrate that corrugation generally enhances light extraction over a wide range of anisotropy factors a , with the exception of structures possessing large aspect ratios combined with low values of a . A linear dependence of extraction efficiency on a is observed, although the slope varies with texture AR . Furthermore, textures with AR values between 0.2 and 0.3 provide the highest extraction efficiencies for $a < 1/3$, whereas for larger anisotropy factors the optimum gradually shifts toward structures with higher aspect ratios.

4 Conclusions

A Floquet-based optical modelling framework for periodically textured OLED structures was presented and validated against large-domain

two-dimensional and three-dimensional simulations. Very good agreement obtained confirms the accuracy of the approach while demonstrating a substantial reduction in computational complexity. The results show that sinusoidal surface corrugations can significantly improve light extraction, with the texture aspect ratio emerging as the dominant geometrical parameter. For isotropic emitters, the highest extraction efficiencies were obtained for aspect ratios around 0.3, whereas the influence of the absolute texture P was found to be comparatively small. Results further show, that texture AR s of approximately 0.2–0.3 is generally optimal for $a < 1/3$, while for highly horizontal orientation ($a \sim 0$), lower AR of ~ 0.1 is preferred. On the other hand, for $a > 1/3$, with more vertical orientation of dipoles, higher AR s provide higher light extraction.

Although the study focuses on blue OLEDs, the underlying optical mechanisms are equally relevant to PeLEDs and other planar light-emitting devices [11]. The presented methodology therefore provides an efficient tool for the design and optimization of nano-corrugated emissive devices with enhanced light-extraction efficiency.

5 Acknowledgments

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Laser-scribed interconnections: from perovskite solar cells to mini-modules

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Abstract: Metal-halide perovskite solar cells (PSCs) have rapidly reached power conversion efficiencies (PCEs) approaching those of established photovoltaic technologies. However, most record efficiencies are demonstrated on small-area devices, while scaling to larger areas remains challenging because of increased coating non-uniformity and resistive losses in transparent conducting oxide (TCO) electrodes [1,2]. A common approach to overcome these limitations is to divide large-area devices into sub-cells connected monolithically in series using P1-P2-P3 laser scribing. Precise control of these laser processes is essential because incomplete ablation can increase contact resistance or cause electrical shunting, whereas excessive laser energy may damage the underlying TCO [2,3].

In this work, nanosecond laser scribing was systematically optimized for the fabrication of inverted p-i-n perovskite mini-modules on $2.5 \times 2.5 \text{ cm}^2$ substrates. Devices were fabricated using the architecture glass/ITO/MeO-2PACz/FA_{0.83}CS_{0.17}Pb(I_{0.83}Br_{0.17})₃/C₆₀/BCP/Cu. Small-area cells with an active area of approximately 0.17 cm^2 were used as reference devices. Mini-modules containing three monolithically interconnected sub-cells were subsequently fabricated with aperture areas of 0.6 and 3.0 cm^2 . The layouts of the small-area cells and the two mini-module designs are shown in Figure 1.

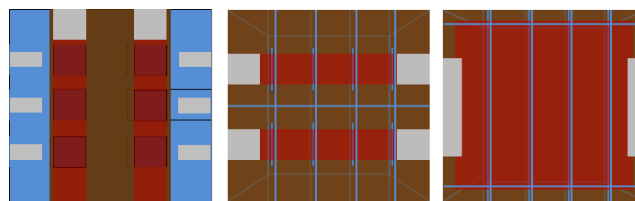


Figure 1: Design of the small-area 6-pixel layout, 0.6 cm^2 , and 3 cm^2 minimodule (L to R).

Laser patterning was performed using a nanosecond Nd:YVO₄ laser. The P1 scribe was produced using a wavelength of 1064 nm to electrically isolate the ITO front electrode, whereas P2 and P3 were performed using 532 nm irradiation. Scanning speed and raster scanning distance (RSD) were systematically varied, and the resulting scribe morphology and elemental composition were examined using scanning electron microscopy (SEM) and energy-dispersive X-ray spectroscopy (EDS).

For P1, low scanning speeds caused excessive thermal accumulation, whereas high scanning speeds resulted in incomplete ITO removal. A scanning speed of 100 mm/s provided clean isolation of the ITO without significant damage to the underlying glass. For P2 and P3, an

RSD of 10 μm produced the most uniform ablation. A smaller RSD of 5 μm resulted in excessive laser overlap and local ITO damage, whereas 20 μm left residual material and, particularly for P3, Cu debris that could potentially cause electrical shunting.

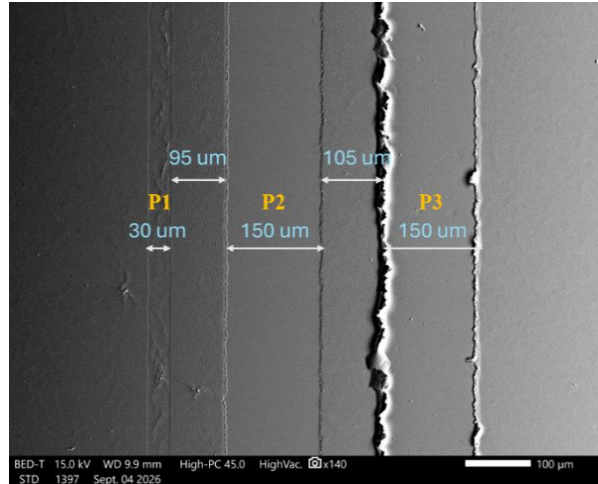


Figure 2: Surface BED-T micrograph of the P1-P2-P3 interconnect region highlighting the individual scribe widths and the total dead width of 530 μm .

Using optimized laser parameters, mini-modules were fabricated. The total P1-P2-P3 interconnection dead width was approximately 530 μm (Figure 2), corresponding to a geometric fill factor (GFF) of 89.4%. The champion 0.17 cm^2 reference cell exhibited a PCE of 18.11%. Upon scaling, the mini-module with an active area of $\sim 0.54 \text{ cm}^2$ retained almost the complete device performance, reaching a champion active-area PCE of 17.87%. The larger mini-module, with an active area of $\sim 2.7 \text{ cm}^2$, achieved 16.09%.

In conclusion, systematic optimization of nanosecond laser scribing combined with SEM and EDS characterization enabled selective P1-P2-P3 ablation while minimizing damage to the underlying ITO. The optimized process preserved nearly the full small-area efficiency during initial scaling, yielding champion active-area PCEs of 17.87% and 16.09% for approximately 0.54 and 2.7 cm^2 mini-modules, respectively. Further improvements in coating uniformity and reduction of the interconnection dead area will be important for extending this approach toward larger-area perovskite modules

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Integration of Temperature and Humidity Sensors into Encapsulated Perovskite Solar Cells

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Abstract: Metal halide perovskites (ABX_3) are gaining significant interest as potential leaders in the next generation of photovoltaics (PV) due to their remarkable optoelectronic characteristics, cost-effectiveness, and ease of production. However, the long-term stability of perovskite solar cells (PSCs) remains a significant challenge, mainly due to substantial degradation when exposed to moisture and oxygen. Therefore, accurate assessment of degradation mechanisms in PSCs requires reliable in-situ monitoring of temperature and environmental parameters directly at the device level. In this work, we present an ultra-thin wireless sensor patch which is designed for fully sealed, in-situ monitoring of encapsulated PSCs. The sensor patch has a footprint of 15×15 mm and an overall thickness of $110 \mu\text{m}$, with electronic components no higher than 0.5 mm. The sensor patch is directly laminated into the encapsulation stack eliminating the need for electrical feedthroughs, thereby preserving the integrity of the encapsulation architecture. The patch integrates temperature, and relative humidity (RH) sensing capabilities, together with a near-field communication (NFC) antenna and readout electronics. This architecture enables both wireless power transfer and data communication via NFC technology. Temperature and RH monitoring are performed using a digital SHT40 sensor, which demonstrates stable operation and reliable data acquisition under NFC-based energy harvesting conditions. To evaluate the environmental durability of the integrated system, damp heat testing is performed under elevated temperature and humidity conditions ($85^\circ\text{C} / 85\%$) in accordance with established stability testing protocols. The outcomes of this sensor-integrated encapsulation platform are expected to support the technological reliability and potential market introduction of perovskite PV technology.

Keywords: Perovskite solar cell; encapsulation; in-situ monitoring; NFC wireless sensing

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1 Introduction

The PSCs are rapidly emerging, achieving power conversion efficiencies (PCE) of 28.0% for single junction and reaching 35.2% for two-terminal (2T) perovskite-silicon tandem solar cells [1]. However, multiple environmental factors, particularly temperature and humidity, obstruct the commercialization of PSCs [2], [3]. Heat or moisture can initiate the release of volatile organic species, leaving

behind lead iodide [4], [5]. Also, the long-term stability of laboratory-scale PSCs critically depends on the effectiveness of encapsulation, as these devices are highly sensitive to oxygen, water vapor, and chemical interactions with encapsulation materials [3], [6]. Accurate assessment of degradation mechanisms in PSCs therefore requires reliable in-situ monitoring of

temperature and environmental conditions at the level of the solar cell itself.

The in-situ measurement of temperature and humidity within encapsulated devices for silicon-based PV modules has previously been conducted using digital humidity sensors that have been connected by wires or wirelessly using radio-frequency identification (RFID) technology [7], [8]. These measurement techniques have demonstrated their value as a useful instrument not only for in-situ monitoring of water concentration in PV modules subjected to accelerated testing conditions within climatic chambers but also for long-term outdoor real-time monitoring in field conditions [9], [10].

The PSCs are generally laminated in glass/glass configuration, where the temperature is typically measured at the external glass surface, which can significantly deviate from the actual operating temperature of the PSCs, particularly under realistic outdoor operating conditions. Embedding conventional wired sensors within the lamination layers is possible but introduces feedthroughs that increase fabrication complexity and may compromise encapsulation integrity.

In this research work, we present an ultra-thin wireless sensor patch that enables fully sealed in-situ monitoring of encapsulated PSCs. The patch integrates an NFC antenna and a readout chip supporting I²C-compatible sensors, with wireless power supply and data transmission provided via near-field communication (NFC). The PSCs were encapsulated between two glass layers using cross-linked Polyolefin Elastomer (POE) as the primary encapsulant, while Polyisobutylene (PIB) serves as the edge sealant. The environmental durability and operational reliability of the sensor-integrated encapsulation architecture were evaluated under accelerated damp-heat conditions of 85 °C and 85% RH, with sensor measurements

recorded at regular intervals throughout the experiment.

2 Experimental

2.1 Perovskite solar cell preparation

PSCs, fabricated for the purpose of this work, have an inverted (p-i-n) planar architecture. A structured ITO-coated glass (Automatic research, $R = 15 \Omega \text{ sq}^{-1}$) served as the substrate, supporting six solar cells, with each solar cell having a final size of 0.17 cm^2 . Before fabrication, the substrates underwent a cleaning process in an ultrasonic bath, which was conducted in four steps, each lasting 12 min. For the cleaning purpose acetone, detergent, deionized water and isopropanol were used. Prior to the spin-coating process, a cleaning procedure lasting 15-min was conducted using ozone and UV light. All stages of the fabrication process are carried out in a nitrogen atmosphere.

After cleaning, a self-assembled monolayer (MeO-2PACz) in an ethanol solution serving as a hole transport layer (HTL) was spin-coated for 30 s at a speed of 3000 rpm, followed by immediate annealing at 100 °C for a duration of 10 min. The Perovskite solution preparation is based on the use of "stock solutions" and adopted from [11]. The 1.5 molar stock solutions of PbI_2 , PbBr_2 and CsI are added to the crystalline FAI , including a 5% excess of PbI_2 . Subsequently, a perovskite layer $[\text{Cs}_{0.17}\text{FA}_{0.83}\text{Pb}(\text{I}_{0.83}\text{Br}_{0.17})_3 + 5\% \text{PbI}_2]$ was applied using spin-coating at a speed of 4000 rpm for a duration of 35 s, while adding ethyl acetate after 25 s of initiating the spin-coating procedure. The samples underwent annealing for 40 min at a temperature of 100 °C. The electron transport layer (ETL) composed of C_{60} (21 nm) is deposited through evaporation in a vacuum chamber, after which the SnO_2 layer (20 nm) is applied using ALD. The copper back contact (100 nm) is made by a further evaporation process, and the device is ultimately finalized by removing the excess

material from the edges and applying the silver front contacts. In the last, all devices were capped with 30 nm of Al_2O_3 using ALD at 100 °C, using Trimethylaluminium (TMA) and water as precursors to prevent moisture ingress and prolong their long-term stability [12].

2.2 Temperature and Humidity Sensor SHT40

The SHT40 (Sensirion) is a digital sensor designed to measure relative humidity and temperature, utilizing Sensirion's fourth-generation SHT4x sensor platform. This sensor integrates humidity and temperature sensing elements with on-chip signal processing and provides calibrated digital measurements via an I²C communication interface. The equations for calculating temperature and relative humidity are given as follows in the datasheet [13]:

$$T = \left(-45 + 175 \times \frac{S_T}{2^{16}-1} \right) ^\circ\text{C} \quad (1)$$

$$\text{RH} = \left(-6 + 125 \times \frac{S_{RH}}{2^{16}-1} \right) \% \text{RH} \quad (2)$$

The SHT40 is housed in an open-cavity dual-flat-no-lead (DFN) package, featuring a humidity-sensitive opening on the top surface and four electrical connections for I²C communication, power supply, and ground. With a compact footprint of approximately 1.5 × 1.5 × 0.5 mm, it is well-suited for integration into miniaturized sensing platforms. The sensor offers a typical temperature accuracy of ±0.2 °C, with a resolution of 0.01 °C across a specified temperature range of −40 to +125 °C. For relative humidity measurements, the SHT40 achieves a typical accuracy of ±1.8% RH, a resolution of 0.01% RH, and operates within a humidity range of 0–100% RH. The typical response times for temperature and humidity are approximately 2 s and 4 s, respectively, as stated in the datasheet [13].

2.3 Sensor patch integrated encapsulation

The fabricated PSCs were encapsulated utilizing a glass-glass configuration. Each

substrate was sandwiched between two pieces of glass measuring 50 mm × 50 mm × 2.0 mm. Cross-linked polyolefin elastomer (POE) films served as the primary encapsulant, with a total of five sheets employed. To prevent mechanical damage to the individual layers within the PSCs stack, three layers of POE are incorporated on the side where the sensing patch is located. The additional POE layer serves as a flexible buffering interface, reducing local mechanical stress and mitigating the risk of damage to the functional layers of the PSC during lamination and device operation. Four layers of PIB having thickness of 0.8 mm and a width of 10 mm (H.B. Fuller, HelioSeal PVS 101), were applied around the perimeter of the glass as an edge sealant to minimize moisture and gas ingress. PV ribbons were connected to the cell contacts using silver conductive paint and routed through the edge sealant.

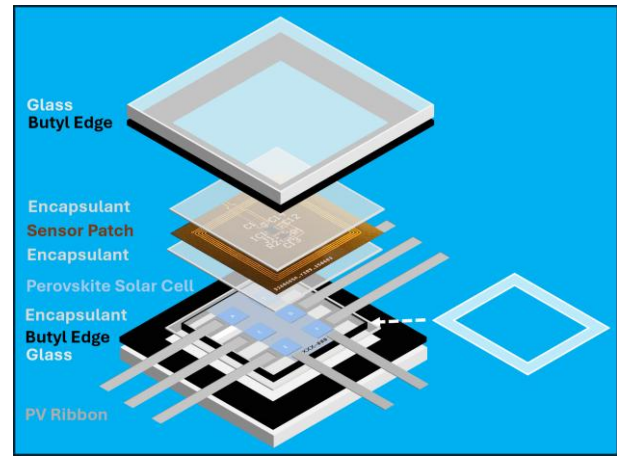


Figure 1: Illustration of sensor patch integrated encapsulation of PSCs.

A metallic frame, measuring 6.8 mm in thickness, was placed around the encapsulation stack to ensure a uniform mechanical load and to minimize deformation of the glass and encapsulant during lamination process. Also, a metallic plate is placed over the cell and frame to ensure that the membrane of the module laminator applies uniform pressure across the entire encapsulation assembly during the lamination process. The assembled package was

subsequently laminated using an industrial-grade module laminator (NPC Incorporated, LM-50 × 50-S) under controlled temperature, vacuum, and pressure conditions. Initially, the chamber was evacuated to its lowest achievable pressure over 8 min and then subjected to pressing duration of 14 min and concluded with a 1-min pressure-retention phase. The lamination temperature was maintained at 145 °C for a total cycle time of 23 min, including the vacuum and pressing stages. Afterward, the chamber was returned to atmospheric pressure, and the encapsulated substrates were removed from the laminator and allowed to cool naturally to room temperature.

2.4 Readout electronics

To achieve wireless readout of the sensor-integrated encapsulated PSCs, an STM32 Nucleo-64 microcontroller platform (Co71RB) was combined with an X-NUCLEO NFC reader expansion board (NFC12A1). The Nucleo platform is responsible for providing embedded processing and control functionalities, while the NFC expansion board, which utilizes the ST25R300 high-frequency NFC reader, enables wireless communication with the NFC-enabled sensor patch [14], [15].



Figure 2: NFC reader.

Communication between the NFC reader and STM32 controller occurs via an SPI interface, which allows for the processing and transfer of the acquired sensor data by the external readout electronics [14]. This configuration enables a contactless readout approach, enabling interrogation of the embedded

sensor patch through its encapsulation without necessitating a direct electrical connection to the external measurement system.

3 Results and Discussion

The final encapsulated PSC incorporating the sensor patch is shown in Fig. 3., with the left and right images displaying the front and back sides, respectively.

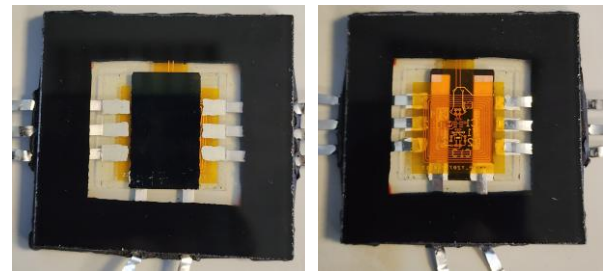


Figure 3: Sensor patch encapsulated PSC.

The front-side view indicates that the lamination process has maintained the visual integrity of the device, with no apparent damage or deformation in the active area. The back-side view clearly reveals the integrated sensor patch within the encapsulation stack. The successful lamination of the sensor-containing structure was achieved without any air bubbles, voids, or delamination, indicating uniform consolidation of the POE encapsulant around the sensor patch. Consequently, the developed integration method enables the sensor patch to be embedded on the rear side of the PSC without visibly affecting the device structure, thereby providing a practical basis for in-situ monitoring within the encapsulated devices.

Fig. 4. Illustrates the temperature and relative humidity measured from the sensor patch encapsulated PSC following prolonged damp heat exposure at 85 °C and 85% RH. The initial measurements prior to exposure were 26.44 °C and 28.29% RH. For each measurement, the device was taken out from the damp heat chamber, and the first reading was recorded immediately after removal. The temperature measured right after removal varied between

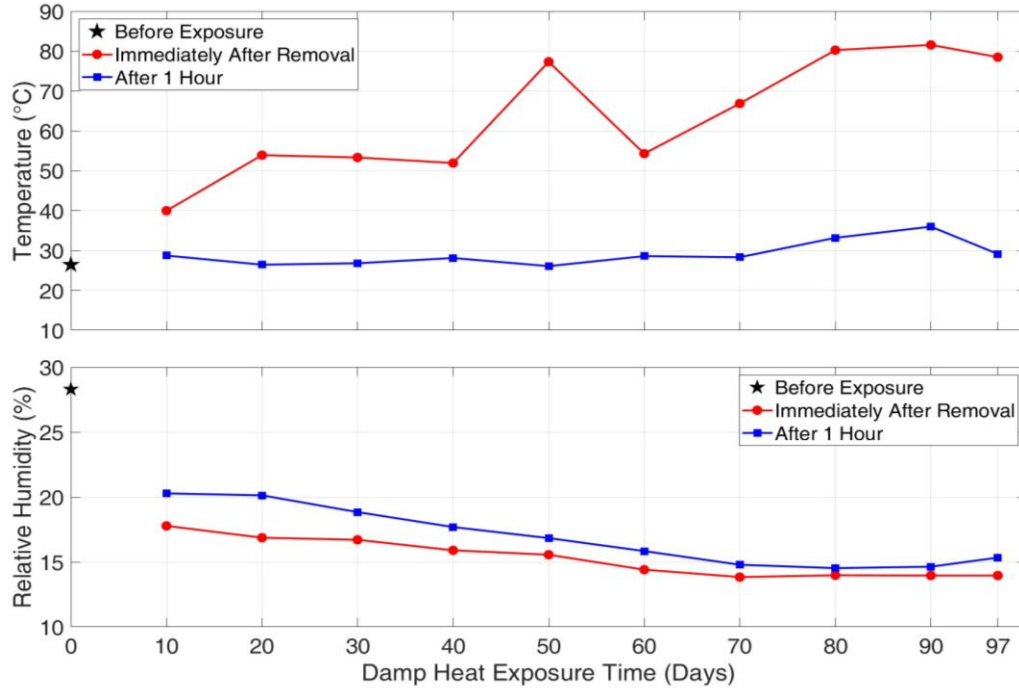


Figure 4: Temperature and relative humidity measured from the encapsulated PSC following damp heat exposure at 85 °C / 85% RH.

39.98 and 81.55 °C, indicating the thermal condition of the device at that moment. The variation in the measured temperature is also affected by the duration needed to transfer the sample from damp heat chamber and commence the measurement.

A significant drop in temperature was observed after allowing the device to stabilize for 1 hour. The temperature decreased to approximately 26–36 °C, nearing the ambient temperature, while the corresponding relative humidity increased from 14–18% immediately after removal to approximately 15–20% after 1 hour. This inverse relationship between temperature and relative humidity aligns with the thermodynamic definition of relative humidity. Relative humidity is defined as the ratio of the actual water-vapor partial pressure to the saturation vapor pressure at the measurement temperature, with the latter being highly dependent on temperature [16].

$$RH = \frac{e}{e_s(T)} \times 100\% \quad (3)$$

Consequently, as the temperature of the encapsulated structure decreases after removal from the damp heat chamber, the saturation vapor pressure also declines,

leading to an increase in the measured relative humidity, assuming the amount of water vapor remains relatively constant. This phenomenon is particularly noticeable in the measurements taken after 1 hour. Thus, the observed temperature and relative humidity response reflects the thermal equilibration of the encapsulated device rather than a sudden alteration in its internal moisture content. These findings illustrate the effective integration of the ultra-thin wireless sensor patch into the completely sealed PSC, facilitating reliable in-situ monitoring of temperature and relative humidity while preserving the integrity of the encapsulation.

4 Conclusions

The presented wireless sensor patch provides a powerful and versatile tool for in-situ monitoring of temperature and relative humidity in encapsulated PSCs. It complements existing measurement techniques while reducing system complexity and preserving encapsulation integrity. This innovation offers significant insights into environmental stress and degradation processes, thereby facilitating the

advancement of more dependable and commercially feasible perovskite PV technology.

Now, the further work will focus on integrating VOC sensing for monitoring outgassing phenomena inside the encapsulated PSCs. Detection of volatile species originating from perovskite layers or encapsulation materials will provide an additional diagnostic parameter for assessing chemical degradation and encapsulant stability, contributing to enhanced reliability assessment and guiding the design of more durable next-generation PV devices.

5 Acknowledgments

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Power Management of Bluetooth Wireless Irradiance Sensors

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Abstract: Accurate irradiance monitoring under dynamic and non-uniform conditions requires multiple sensors with a high sampling rate. Wireless sensors are well suited for this purpose, as they allow flexible installation while avoiding extensive cabling. However, wireless sensors come with their own set of challenges, mainly power and synchronization. In the case of wireless irradiance sensors, an attractive power source is solar power itself. With careful design, the reference solar cell can be used both as a measuring device and a power source. This requires an energy harvesting circuit capable of powering the system from a reference solar cell. Here, the challenge is the low output voltage of the cell, especially while not operating under direct sunlight. The energy harvesting circuit must also support frequent disconnection from the cell, to not interfere with the irradiance measurements. Synchronization of wireless devices is also challenging, due to the limited accuracy of their crystal oscillators, which inevitably drift apart, requiring frequent re-alignment. In this work, we focus on the requirements for a reference cell and a power management system that would enable a wireless irradiance sensor to operate self-sustainably in dynamic outdoor conditions. We measured the power consumption of a prototype sensor design and simulated transient behavior of a 2 cm² IBC reference solar cell to determine the available power and the effects of frequent switching on power extraction and measurement accuracy. The results show that the cell can support full speed sensor operation at irradiances above 139 W/m², and by reducing the sampling rate, operation can be sustained down to 49 W/m².

Keywords: Bluetooth Low Energy, distributed sensors, power consumption, synchronization

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1 Introduction

Transportation is one of the most important aspects in our everyday lives. While it is still majorly reliant on fossil fuels, rising fuel prices are promoting adoption of sustainable mobility [1]. As the price of photovoltaics continues to fall, it is becoming increasingly viable to integrate them in locations that are not normally considered optimal [2]. One such location is on vehicles, a research field called Vehicle Integrated Photovoltaics (VIPV) [3]. The operation of solar cells and panels is typically

monitored using maximum power point trackers and current-voltage (I-V) curve scanners. At the same time, the solar irradiance is monitored using temperature compensated reference sensors. Compared to static PV installations, the irradiance exhibits rapid changes during vehicle movement, caused by the relative motion of the surrounding environment [4], [5]. Another challenge is the non-uniformity of irradiance across the vehicle's surface. To accurately monitor such conditions, a fleet of many sensors with a high sampling rate is required [6]. Using wireless sen-

sors for this application allows simplified installation and removes cable clutter. One of the main challenges in such wireless sensors is battery life. Ideally, the sensors would be self-sustainable, getting power from an onboard generator.

A good example of a system of distributed BLE wireless sensors is the Aerosense system [7]. It is a system of self-sustainable sensor nodes for use on wind turbines. Each node contains sensors such as barometers, microphones and differential pressure sensors. The nodes are installed on rotor blades and transmit the data to a nearby base station. The sampling rates of sensors differ, ranging from 100 Hz all the way up to 16 kHz. Due to the high amount of data, both lossy and lossless compression are applied before transmitting data. With an active power consumption of 140 mW and an average consumption of 10 mW, the authors state that the system can be self-sustainable in the UK for 95 % of days in the year using an 800 cm² solar panel.

2 Materials and Methods

In this paper we propose a self-sufficient wireless irradiance sensor system using a single solar cell, depicted in Figure 1.

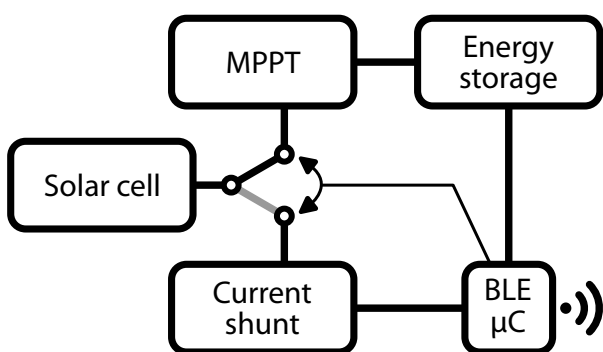


Figure 1: Proposed sensor architecture: A 2 cm² IBC solar cell, a 330 mΩ measurement shunt, an energy harvesting circuit with MPP tracking, a battery or a super-capacitor energy storage and a BLE-capable microcontroller.

We followed the idea that, for irradiance sensors based on reference solar-cell measurements, the same solar cell could also be used

to power the sensor. When designing such a circuit, it is important to consider the energy lost during measurement, and conversely, the effect of switching between maximum power point (MPP) and the irradiance measurement operation, usually done at short circuit (SC) conditions. Modern high-efficiency PV cell technologies feature higher conversion efficiencies but also longer free-carrier lifetimes, which increase the diffusion capacitance [8]. Consequently, applying the short-circuit condition introduces a current transient, which leads to measurement errors if the current is sampled too soon.

The sensor architecture is based on the Nordic Semiconductor nRF54L15 platform, while the receiver base station uses the nRF54LM20A chip, for its native USB capabilities. The nRF54 series is particularly suitable for fast sampling distributed sensors, thanks to their low power consumption, and due to a built-in 52-bit GRTC timer with a resolution of 1 µs [9]. The timer is used by the BLE link-layer, as well as being accessible to the application layer. This enables easy synchronization of actions such as sampling between devices, using the AnchorSync method. It also features a 10-bit ADC, capable of sampling up to 2 Msps and using hardware oversampling to achieve higher resolution. The sampling of the ADC can be triggered directly by the GRTC using the peripheral interconnect feature, ensuring synchronous sampling across all devices.

The first prototypes were implemented using the nRF54L15DK development boards. The boards feature power separation of debug circuitry, enabling accurate power consumption measurements. To assess power consumption, the basic functionality of the sensors was implemented as follows: The ADC peripheral was configured to perform differential measurements. The AnchorSync method was implemented in the firmware of both the sensor nodes and the receiver node. The ADC was configured for sampling at a frequency of 1 kHz, synchronized to the receiver's clock.

This enables synchronous sampling in all connected sensor nodes. The sampled data was continuously transmitted over BLE to the receiver. The total conversion time for every sample was 336 μ s.

To determine the energy requirements, power consumption was measured while the sensor was performing sampling and transmitting data. The measurements were done using a Joulescope JS110 analyzer. When compiling the firmware, special attention was paid to disabling any unused features and peripherals that would unnecessarily increase power consumption. The power measurement was done first at the full sampling rate of 1 kHz, and then at progressively lower sampling rates, to determine the relationship between sampling rate and power consumption. An additional measurement was done with the ADC peripheral disabled, to determine its base power consumption.

To simulate the transient events of the reference solar cell, the parameters for an IBC cell with an area of 2 cm² were chosen for simulation, as this corresponds to a reference solar cell that is already used in the laboratory. In the simulation, the cell was switched between irradiance measurement using a 330 m Ω shunt and the MPP, implemented using a resistor value corresponding to I_{MPP} and V_{MPP} . Based on the duration of the transient events, and the ADC conversion time, the minimum required measurement duty cycle was determined. By also varying the irradiance, the minimum irradiance that still supported the full sampling rate was determined. The derating of sampling rate was also examined, by determining the available power at reduced sampling rates.

3 Results

While sampling and transmitting data, the average power consumption of one sensor node was 3.17 mW. Power consumption is highly periodic, repeating every 50 ms, which is the interval between BLE connection

events. The power consumption in one connection interval is shown in Figure 2. The peaks at the start are packets being exchanged by the sensor and the receiver.

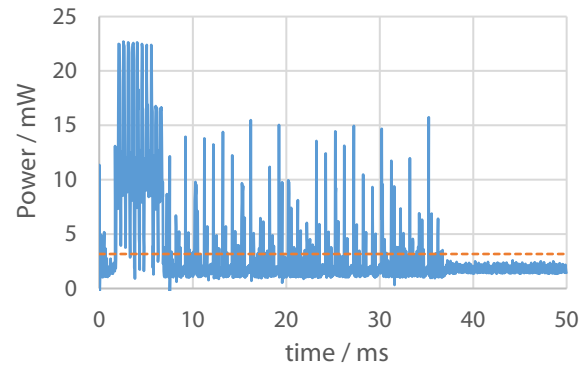


Figure 2: Power consumption in the period of one connection interval, the dashed line represents the average power consumption of 3.17 mW.

The correlation between the sampling rate and power consumption is shown in Figure 3.

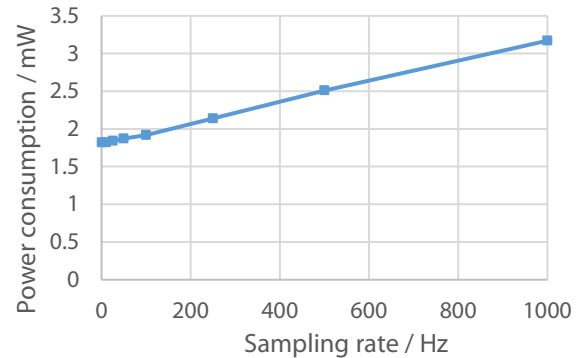


Figure 3: Power consumption vs. sampling rate

A linear correlation is visible, with a base power consumption of 1.80 mW, and a sampling rate dependent additional consumption of 1.37 μ W/Hz. After disabling the ADC peripheral completely, the power consumption decreased to 492 μ W, indicating a base ADC power consumption of 1.31 mW.

3.1 Transient simulation

The reference solar cell has an I_{SC} of 76.2 mA and a P_{MPP} of 43.1 mW. SPICE simulations showed that when switching the solar cell from MPP to measurement, there is a current spike of up to 1.6 A that lasts 4.6 μ s, caused by

the cell's high diffusion capacitance. The time plot of the transient event is shown in Figure 4. Based on the results of this measurement, a delay needs to be introduced after switching and before ADC sampling. Choosing a safe value of $10\ \mu\text{s}$, the total conversion time is increased to $346\ \mu\text{s}$, giving a measurement duty cycle of 34.6 % at a 1 kHz sampling rate.

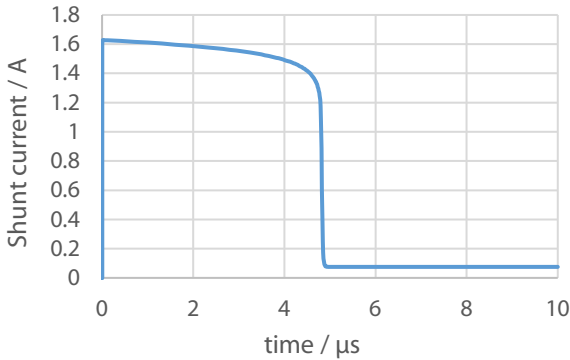


Figure 4: Shunt current immediately after switching from MPP to measurement

3.2 Energy budget evaluation

Simulating the minimum measurement duty cycle, the average power output of the solar cell drops to 25.4 mW, which is approximately 8 times more than required for sensor operation. The minimum irradiance at which the cell still provides 3.17 mW of power is $139\ \text{W}/\text{m}^2$. At lower irradiances, the diffusion capacitance also decreases, making the transient events shorter. In the case of minimum irradiance, the transient event duration was less than 600 ns, however, since the total conversion time is dominated by the ADC delays, the $10\ \mu\text{s}$ conversion delay was not changed.

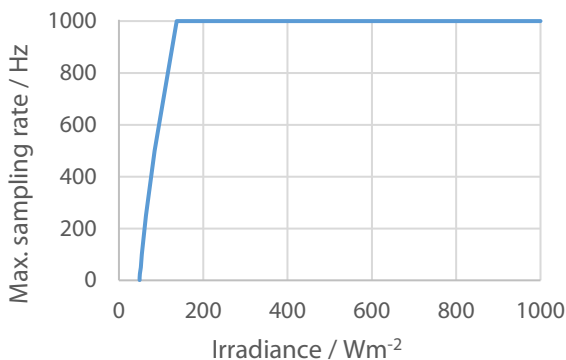


Figure 5: Maximum sampling rate vs irradiance

The derating of sampling rate is shown in Figure 5. The minimum irradiance that still supports the base sensor consumption is $49\ \text{W}/\text{m}^2$.

4 Conclusion

Wireless sensors are a good fit for use in VIPV research, enabling easy and versatile installation. To test our proposed concept, we have developed prototypes to measure power consumption during operation. The prototypes contain all the main components, so the energy requirements are accurately captured. A clear linear correlation between power consumption and sampling rate is visible. As the sampling rate decreases, the ADC peripheral uses less power, and the number of BLE packets is also reduced. At very low sampling rates, power consumption is effectively equal to the base consumption of the sensor, of which the largest part is the static consumption of the ADC.

The simulated cell closely matches the specification of the real reference cell. A $2\ \text{cm}^2$ IBC solar cell, with a P_{MPP} of 43.1 mW, provides only 25.4 mW, when switched between measurement and MPP with a duty cycle of 34.6 %. MPP power doesn't scale linearly with irradiance, so the minimum irradiance at which the sensor can still operate at full sampling rate is only 7.2 times lower, at $139\ \text{W}/\text{m}^2$. By reducing the sampling rate, power consumption is decreased, and cell power available for MPPT is increased. This allows for reduced operation at even lower irradiances, down to $49\ \text{W}/\text{m}^2$.

Future work will focus on further optimization of power consumption and self-sustainability. Power consumption can be reduced by utilizing modern BLE protocol features such as 2 Mbps PHY speed, which reduces the transmission time and data packet length extension, which reduces the overhead of splitting data into multiple packets. There is also the option of reducing the total ADC conversion time, which is currently dominated by the ac-

quisition period. By providing a low impedance source to the ADC inputs, the acquisition time could be reduced without sacrificing accuracy, which in turn would allow for more energy to be extracted from the cell and used for power.

5 Acknowledgments

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Fast Bidirectional IV Curve Acquisition of High-efficiency PV Modules

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Abstract:

The rapid development of photovoltaic (PV) technologies has increased the need for accurate and fast electrical characterization of PV modules. Current-voltage (*IV*) curve measurements provide essential information about PV performance, but fast acquisition can introduce measurement errors, particularly in case of high-efficiency (HE) modules, which exhibit increased capacitive effects. This work presents a software-controlled *IV* curve acquisition system based on a conventional electronic load and an external 16-bit simultaneous-sampling analog-to-digital converter (ADC). The system uses an STM32G4 microcontroller to control a linear power MOSFET and acquire synchronized measurements of module voltage, current, and irradiance through an AD7606B ADC. A configurable *IV* scanning algorithm enables scan durations ranging from 15 ms to several seconds while allowing different scanning parameters and directions. The developed system was evaluated using simulated PV modules and real PV modules under clear-sky conditions. Measurements demonstrated that rapid bidirectional scanning introduces hysteresis associated with capacitive effects, with the strongest dynamic behavior occurring near the maximum power point (MPP). Comparison between a conventional crystalline-silicon module and a high-efficiency TOPCon module showed substantially stronger hysteresis in the latter at short scan durations. The results highlight the importance of considering capacitive effects, scan direction and duration when performing fast *IV* measurements and demonstrate the suitability of the proposed system for configurable PV characterization under dynamic operating conditions.

Keywords: Photovoltaics; Fast *IV*; Software-controlled

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1 Introduction

Photovoltaic (PV) technologies experience rapid growth, driven by the increasing demand for renewable energy and continued improvements in PV cell and module technologies. Advances in materials, cell architecture, manufacturing processes, and economies of scale have contributed to increased PV performance and have supported widespread deployment in both distributed rooftop systems and large-scale photovoltaic power plants.

As PV deployment continues to expand and module technologies evolve, accurate characterization of PV performance under different operating conditions becomes increasingly important. Among the available characterization methods, the current-voltage (*IV*) curve characterization represents the basic evaluating technique to determine the electrical performance of a PV module. The *IV* characteris-

tics provides information about important parameters such as the open circuit voltage, short circuit current, maximum power point, and fill factor, while deviations from the expected characteristic can also provide information about module performance and potential faults. *IV* measurements are therefore used not only for research and characterization, but also in PV system installation, commissioning, maintenance, and troubleshooting.

2 Related Works

Accurate *IV* characterization requires sufficiently stable irradiance and temperature throughout the measurement. Under changing outdoor conditions, variations during the scan can distort the reconstructed curve, making acquisition time an important parameter. Consequently, various *IV* tracer topologies and acquisition methods have been investigated to reduce measurement time while maintaining accuracy [1], [2], [3].

The need for fast *IV* curve acquisition becomes more challenging with the increasing adoption of high-efficiency (HE) PV technologies such as PERC, TOPCon, IBC, and HIT, which can exhibit pronounced capacitive behavior associated with long minority-carrier lifetimes and increased diffusion capacitance. During rapid *IV* scanning, these effects can cause deviations from the quasi-static current response and distort the measured *IV* characteristic. Consequently, faster scanning does not necessarily improve accuracy, with errors of up to 4% in the measured maximum power point reported for HE modules. Algorithmic compensation has been shown to reduce these errors to below 1%, highlighting the importance of both the scanning hardware and the acquisition algorithm [4].

In this paper, we present a software-controlled *IV* curve acquisition system using a MOSFET based electronic load and an external 16-bit simultaneous sampling analog to digital con-

verter (ADC). Attention is given to the configurability of the measurement hardware and the *IV* scanning algorithm, allowing the scanning strategy to be adapted to different measurement conditions and PV technologies.

3 Design and development

3.1 System Architecture

The proposed system is based on an STM32G4 microcontroller [5], which is responsible for system control, load regulation, data acquisition, and communication. By controlling the MOSFET, the operating point of the PV module can be varied over its *IV* characteristic. Figure 1 presents the block diagram of the system.

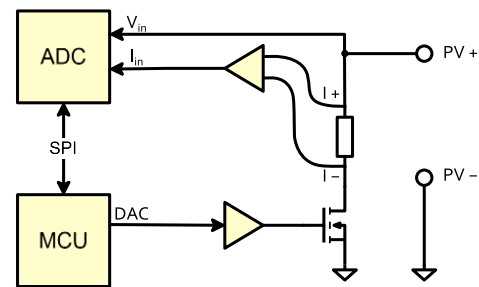


Figure 1: Block diagram of the implemented system.

3.2 Electronic Load

The electronic load consists of a DAC, an operational amplifier, and a power MOSFET. The hardware is designed to accommodate PV modules with operating voltages ranging from approximately 0.7 V, corresponding to a single PV cell, up to 60 V. This wide voltage range is achieved by amplifying the DAC output voltage from its native range of 0–2.5 V to 0–10 V. The resulting gate-drive voltage provides sufficient control range for the MOSFET over the specified PV voltage range.

The selected IXTK90N25L2 is a linear power MOSFET designed for operation in its linear region. Its safe operating area (SOA) makes it suitable for the voltage, current and pulse duration conditions encountered during *IV* scanning [6]. During operation, the MOSFET acts

as a variable load, with its conduction controlled by the amplified DAC signal. Consequently, the load can be continuously adjusted to move the PV module operating point across its IV characteristic.

3.3 Measurement ADC

The sensing component of the system is based on the AD7606B, a 16-bit simultaneous-sampling ADC with eight bipolar input channels and sampling rates of up to 800 kSPS [7]. The measured signals are processed by the microcontroller and used by the control algorithm to adjust the DAC output and, consequently, the operating point of the PV module. The ADC also provides selectable input ranges, allowing signals with different amplitudes to be acquired.

Its simultaneous sampling capability is particularly relevant for fast IV acquisition, as the voltage, current, and irradiance signals can be acquired using a common sampling reference. This eliminates the temporal offset associated with sequential sampling and provides direct correspondence between the electrical operating point and the irradiance conditions during the scan.

3.4 IV Scanning Algorithm

The implemented hardware provides a high degree of configurability, allowing the DAC and external ADC to operate together or independently. This enables different IV scanning strategies without hardware modifications. Here, we propose a baseline IV curve scanning algorithm, that will allow us to evaluate the measurement system and provide a reference for future development and evaluation of different scanning strategies.

Since scan duration affects measurement accuracy due to diffusion capacitance, the algorithm provides a defined and repeatable scan duration. Before acquisition, the user-defined parameters are set, including the number of voltage and current points, scan duration,

oversampling ratio (OSR), scan direction, and unidirectional or bidirectional operation. The algorithm then measures the open circuit (OC) voltage (1) and short circuit (SC) current (2) to define the voltage and current steps, determined by the predefined number of IV points. Based on the SC and OC values, the start and stop DAC voltages of the sweep are determined. This is necessary because the MOSFET is a non-linear device that exhibits linear-like behavior only within a specific gate voltage range, which mainly depends on the drain-source voltage V_{DS} and temperature.

First, the MOSFET gate is driven to the highest voltage to reach the SC conditions. Then the stop DAC voltage is determined by decreasing the MOSFET gate voltage, until the PV module voltage value rises to reach 1% of the measured V_{OC} (3). The algorithm then drives the MOSFET to the lowest voltage reaching OC conditions and continues in the same manner to determine the starting point (4). The DAC then incrementally sweeps between start and stop DAC voltages (5) while simultaneously acquiring voltage and current and storing only the IV points that fulfill the predefined point density conditions. After DAC reaches the end voltage, the data acquisition continues until the PV module reaches SC point to account for delays caused by PV module dynamics. The algorithm then waits for the transients to settle before terminating or reversing the scan direction for bidirectional operation (6). The algorithm is depicted in Figure 2.

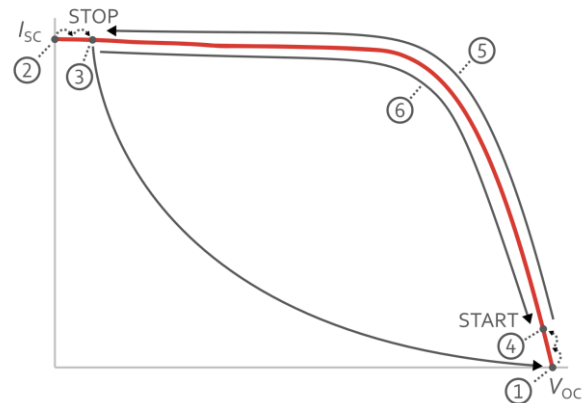


Figure 2: Step-by-step operation of the IV curve algorithm.

4 Results

To best evaluate the performance of the developed IV curve scanning system, we carried out experimental measurements first on a solar array simulator (SAS), followed by outdoor measurements on a clear sky day.

4.1 Solar Array Simulator Results

For the initial testing we chose different modules which were simulated on the Agilent E4350B Solar Array Simulator. The modules ranged from low voltage and high current to higher voltage and medium current, reaching higher power ratings.

The initial results show that the developed IV scanning device can capture high-quality IV curve data. The implemented algorithm supports IV scan durations from as low as 15 milliseconds to 10 seconds or more. Zoomed IV curves with different durations of 18, 50, and 200 ms of a simulated PV module ($V_{oc} = 44$ V, $I_{sc} = 8$ A) are shown in Figure 3. It is evident that the output capacitance of the SAS causes hysteresis of the IV curve, which is more evident at short scan times. The P_{MPP} measurement results of all the bidirectional IV curve scans are represented in Table 1 for comparison.

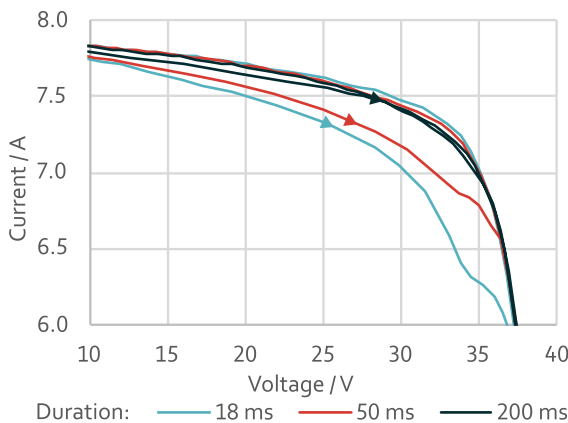


Figure 3: Zoomed IV curves of the simulated PV module acquired with different scan durations.

Due to the high output capacitance of the SAS, fast IV curve scans introduce transient behavior in the measured output voltage and

current. This behavior is similar to the capacitive effects observed in HE PV modules during rapid IV measurements, where the capacitive current component increases with the voltage slew rate dV/dt [4].

During the IV curve scans all electrical quantities were additionally acquired using an oscilloscope (Keysight MXR258B), enabling time-domain analysis of the measurement. From the acquired data, the voltage derivative dV/dt was calculated for the 18-millisecond scan and plotted together with the measured power as a function of time, as shown in Figure 4.

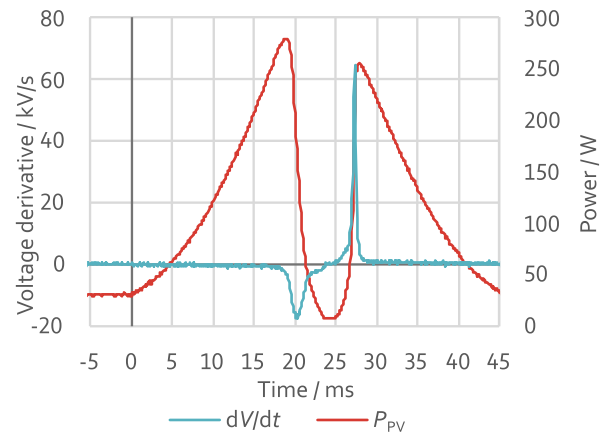


Figure 4: Power and voltage derivative vs. time – SAS PV module.

The voltage derivative provides an indication of the magnitude of the transient component associated with the capacitive behavior of the SAS. By overlapping the voltage derivative and power time series, it is evident that the local minimum and maximum of dV/dt during the bidirectional IV curve scan occur within the region of the maximum power. Since the magnitude of the capacitive current component increases with the voltage slew rate, the measurement error associated with the capacitive behavior is expected to be largest in this region [4].

The results indicate that the largest dynamic measurement error is expected near the maximum power point (MPP), where it can significantly affect the calculated P_{MPP} and the evaluated module performance.

4.2 Outdoor results

Two PV modules were selected to investigate to which extent the dynamic effects influence the fast acquired IV characteristic of actual PV modules, measured outdoors under steady-state clear-sky conditions. We have chosen two distinct technologies, the first being an older low-efficiency Back Surface Field (BSF) crystalline silicon as a reference, where low diffusion capacitance is expected. On contrast, the second PV module was a HE TOPCon PV module representing a state-of-the-art technology. The comparison of the IV characteristics of the two modules will show us additional insight into the influence of the diffusion capacitance on fast IV curve scanning.

Here, the IV curves of both modules were acquired using different scan durations of 18, 50, and 200 ms. Magnified views of the measured IV curves near MPP, where the hysteresis effect is most pronounced are shown in Figure 5.

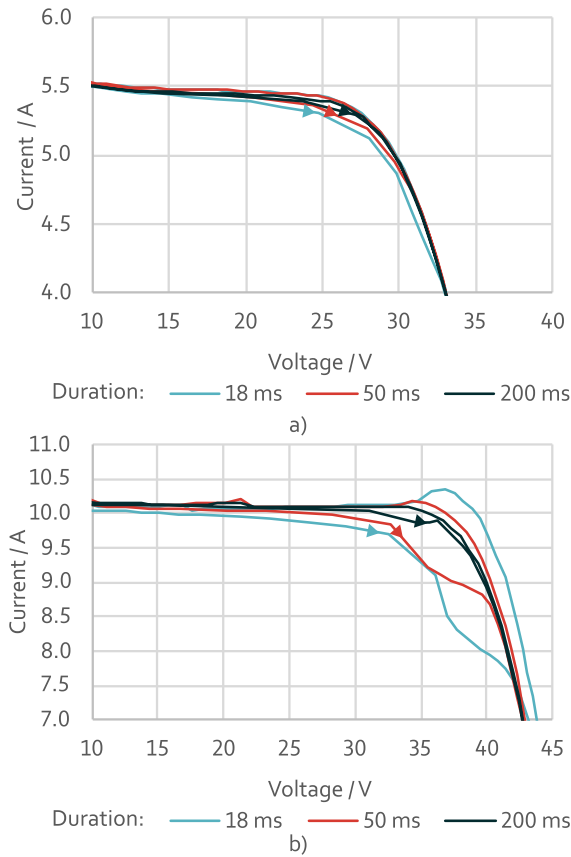


Figure 5: Zoomed IV curves acquired with different scan duration a) BSF crystalline silicon PV module, b) HE TOPCon PV module.

Differences between the forward and reverse scans can be observed in all cases. The hysteresis region is relatively narrow for the investigated BSF crystalline-silicon PV module, indicating a comparatively small influence of capacitive effects under the investigated conditions. In contrast, the TOPCon module exhibits substantially wider hysteresis, particularly at the shortest scan duration, indicating stronger capacitive effects during rapid IV scanning. These results demonstrate that high diffusion capacitance of HE PV modules can severely limit the minimum achievable scan time to keep the measurement error sufficiently low.

In the magnified IV curves of the TOPCon PV module, two additional smaller bumps can also be observed in the flat region towards SC at approximately 14 V and 22 V. We assume that these features are related to the solar cell short circuit current mismatch within the individual substrings of the PV module, as the bumps occur around expected voltages, at which the bypass diode switching occurs. However, the origin of these features requires further investigation and experimental confirmation.

For the TOPCon HE PV module, the electrical quantities were additionally measured using an oscilloscope to investigate the time-domain behavior and calculate the voltage derivative, shown in Figure 6.

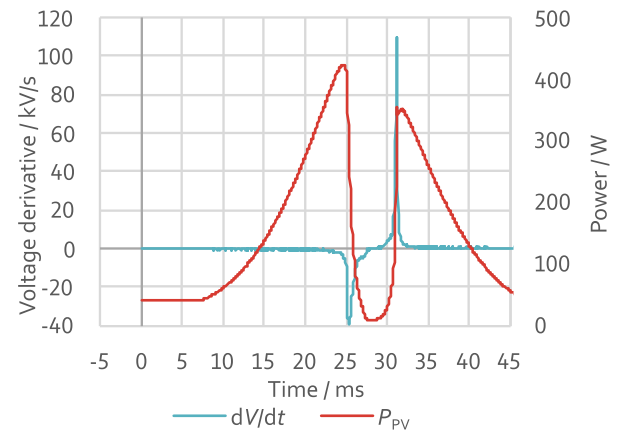


Figure 6: Power and voltage derivative vs. time – HE TOPCon PV module.

Overlapping the two signals reveals behavior similar to that observed with the solar array simulator. The local minimum and maximum of the voltage derivative, corresponding to the two directions of the bidirectional IV scan, occur near the MPP. As discussed previously, a higher voltage slew rate results in a larger capacitive current component and can therefore contribute to additional measurement errors. The results consequently indicate that the region around the MPP is particularly susceptible to dynamic measurement errors during fast IV curve acquisition.

Table 1: PV module IV curve scan duration MPP comparison.

PV module	Scan duration [ms]	P_{MPP} reverse [W]	P_{MPP} forward [W]
Simulator	18	246.26	222.59
44 V 8 A	50	245.58	239.07
244 Wp	200	244.79	244.29
UPSOLAR	18	149.11	145.01
UP-M185M	50	148.91	147.12
185 Wp	200	148.46	148.34
Trinasolar TSM	18	391.55	320.78
435NEG9R.28	50	373.9	350.31
435 Wp	200	367.13	363.71

5 Conclusion

This work demonstrated a configurable IV curve acquisition system capable of scan durations down to 15 ms, with synchronized measurement of PV voltage, current, and irradiance. Experimental results confirmed that fast scanning introduces capacitive hysteresis, with the strongest dynamic effects occurring near the maximum power point.

The comparison between conventional BSF crystalline-silicon and HE TOPCon modules showed a technology-dependent difference in response. The TOPCon module exhibited substantially stronger hysteresis at short scan durations. These results demonstrate that meas-

urement speed cannot be considered independently of PV technology and its dynamic electrical behavior.

The developed system provides a flexible platform for investigating fast IV characterization and establishes a basis for further development of adaptive scanning strategies and capacitive-effect compensation. Such approaches could enable faster measurements while maintaining the accuracy required for reliable PV performance evaluation.

6 Acknowledgments

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7 References

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Electrical modelling of High Efficiency PV modules using Spice

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Abstract: The current-voltage (*I*/*V*) curve is one of the most important characteristics of a PV module. It is usually measured over a relatively short period of time, which tends to introduce measurement artifacts, especially when scanning modern high efficiency (HE) PV modules. Many of the features seen in such *I*/*V* curve scans cannot be explained by lumped single diode models. In simplified models all cells are expected to operate uniformly under a single set of global operating conditions, this assumption is suitable and correct for slower scanning times. At faster scanning rates a model that resolves cell-to-cell interactions is required. In this work we develop a simulation model capable of reproducing such measurement artifacts. The core of the model is based on uneven short circuit currents and operating conditions at photovoltaic cell level. This paper presents a sensitivity analysis of the critical parameters responsible for these artifacts, laying the foundations for future research.

Keywords: Diffusion capacitance; Junction capacitance; PV module; SPICE simulations

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1 Introduction

Throughout the entire lifespan of a photovoltaic (PV) module, its current-voltage (*I*/*V*) curve is repeatedly monitored. First, when assembled in the factory, it is binned according to a measurement of its maximum power point. Second, it is measured again before operational permits are granted for the power plant. Third, once in operation, its performance is regularly checked by performing periodic *I*/*V* curve scans. This chain of measurements and performance evaluations only works if the measurements are reliable and repeatable. Today, most of the newly installed PV modules are so-called high-efficiency (HE) modules. Technologies such as TOPCon, HIT and IBC all feature high power conversion efficiencies together with high diffusion as well as junction capacitances [1]. Because of portability and power dissipation requirements

the *I*/*V* curve scans are limited in duration; which often results in non-negligible measurement artifacts, especially when using the load capacitor measurement method. Current research focuses on corrective algorithms that minimize the overall measurement artifacts and the resulting measurement error [2], [3]. The success of such algorithms is directly tied to the underlying simulation model. Almost all existing work simulates the PV module with a lumped single diode model which assumes uniform operating conditions across the module's surface.

In this paper we focus on simulation models capable of reproducing real measurement artifacts by accounting for uneven operating conditions across the module. We developed a SPICE model and performed a sensitivity

analysis, which gave us valuable insight into the effect of each parameter on the simulated I/V curve scan.

2 Dynamic SPICE model.

A real PV module consists of cells connected in series and grouped into substrings that share a common protection diode. Cells within the substring don't necessarily share a common operating point due to partial shading, light reflections, active area variations and other process uncertainties. Our simulation model therefore adopts a substring-level modelling approach. The substring model, presented in figure 1, consists of two cell groups connected in series. The groups HIGH and LOW as the name suggests have different short circuit currents. Due to the different short circuit currents the LOW group can be pushed into reverse bias. At sufficiently high reverse bias the $D_{SC_LOW_REV}$ starts conducting as the LOW group enters the breakdown region. Every PV substring is protected with a bypass diode D_{BYPASS} .

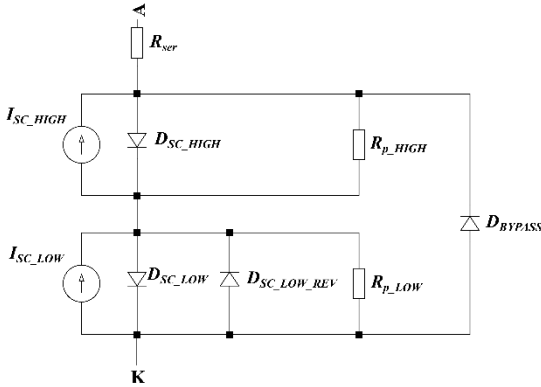


Figure 1: Simulation model of PV substring

A PV module usually consists of 3 or more PV substrings protected with their own bypass diode [4]. Our PV model presented in figure 2 consists of 4 individual in series connected substrings.

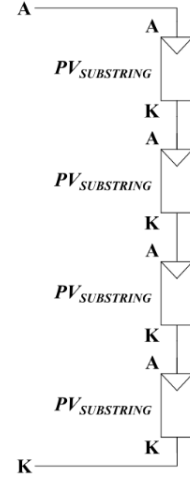


Figure 2: Simulation model of PV module

To obtain I/V curve data we need to simulate a capacitive I/V curve scan. In addition to the described PV module model, we introduce a load capacitor C_{load} with its internal series resistance R_{load} and a switch S_{SC} . The simulated I/V curve scan begins as soon as the S_{SC} is released. The complete simulation circuit is presented in figure 3.

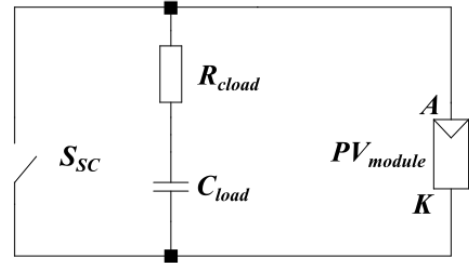


Figure 3: Simulation model of I/V curve scanner.

The default simulation parameters are listed in table 1. The selected values represent a HE PV module with realistic junction and diffusion capacitances. We implemented two realistic load capacitors, one representing a slow and the other representing a faster I/V scan. Alongside these standard parameters we introduced three additional ones: MF , V_{REV} , RHL , which will be explained in detail in sections 3.3, 3.4 and 3.5.

Table 1: Default simulation parameters.

Parameter & description		Value
PV module		
I_{S0}	Nominal reverse saturation current	2.85 nA
N_N	Module-diode ideality factor	88

N_{CELL}	Number of solar cells	80
$N_{SUBSTRING}$	Number of bypass diodes	4
I_{SC}	Short circuit current	10 A
MF	Match factor	4 %
C_{T0}	Junction capacitance of a single solar cell at zero bias	1 μ F
τ	Minority charge carrier life-time	1 mS
R_{SER}	PV modules' series resistance	0.4 Ω
R_{PAR}	PV modules' parallel resistance	4 k Ω
V_{REV}	Breakdown voltage of a single solar cell	10 V
RHL	Ratio High Low	20
Bypass diode		
I_{S0}	Nominal reverse saturation current	436 μ A
N	Diode ideality factor	1
R_S	Series resistance	10 m Ω
C_{J0}	Junction capacitance of a bypass diode at zero bias	1 nF
τ_b	Minority charge carrier life-time of the bypass diode	1 ps
Fast IV curve scanner		
C_{LOAD}	Load capacitance	1 mF
R_{LOAD}	Load resistance	0.1 Ω
Slow IV curve scanner		
C_{LOAD}	Load capacitance	100 mF
R_{LOAD}	Load resistance	0.1 Ω

Using the default parameters, the proposed simulation model produces the baseline simulated IV curves for two capacitive loads, as presented in figure 4. For the slow scan, the load capacitance is selected to obtain a sufficiently long IV scan, during which the dynamic effects of the PV module can be considered negligible. In contrast, the fast scan capacitance is sufficiently low for dynamic effects to become significant, resulting in substantial distortion of the IV curve, especially in the vicinity of the MPP.

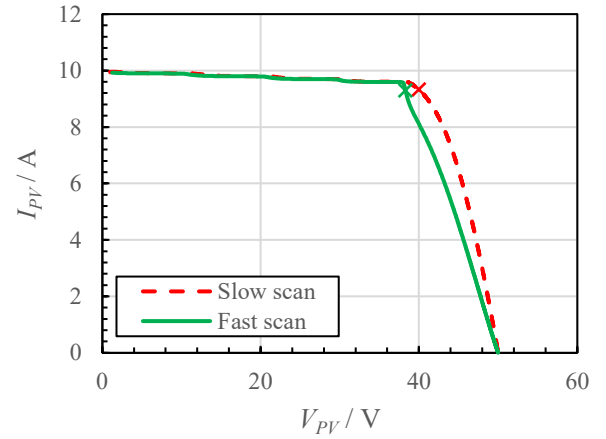


Figure 4: Simulated default IV curve with marked MPP.

3 Sensitivity analysis results

Fitting a simulation model onto the measurement requires sensitivity studies for each parameter. Effects of classic solar cell parameters such as diode ideality factor N_N , series resistance R_{SER} as well as parallel resistance R_{PAR} have been studied before and are not the focus of this work. We will focus exclusively on parameters that distort the IV curve scans mainly at rapid scans: junction capacitance C_{T0} , minority charge carrier lifetime τ , mismatch factor MF , reverse breakdown voltage V_{REV} , and uniformity of mismatch RHL .

3.1 Junction capacitance C_{T0}

First, we tested the effect of junction capacitance as one of two main solar cell dynamic parameters. At values much smaller than the load capacitance, it tends to have minimal to no visible effects, while larger junction capacitances can drastically distort the IV curve right at the P_{MPP} . This observation is visible both on the simulated IV curves presented in figure 5 as well as on the extracted P_{MPP} presented in figure 6.

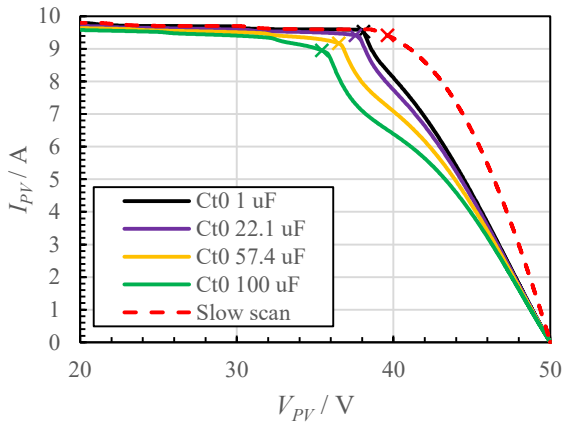


Figure 5: Effects of junction capacitance on the simulated I/V curves.

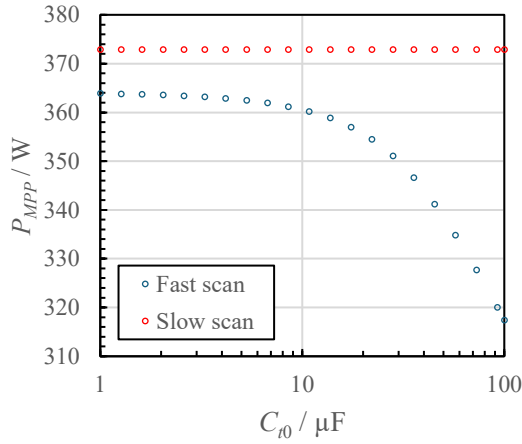


Figure 6: Effects of junction capacitances on the simulated P_{MPP} .

3.2 Minority charge carrier lifetime τ

The junction capacitance is usually dominated by the diffusion capacitance, when approaching the MPP and beyond. The diffusion capacitance is governed by the minority charge carrier lifetime τ , which is especially long in high efficiency solar cells. Its effect on the simulated I/V curve is presented in figure 7. For lifetimes τ up to a few $10 \mu s$, the measurement error is not detectable. However, in modern HE solar cells, lifetimes of a few $10 ms$ can be expected [5], where the distortion is severe along the whole I/V curve from the MPP towards the V_{OC} . Interestingly, in figure 8 we can observe that the overall P_{MPP} decreases only slightly up to relatively high minority charge carrier lifetimes, even though visible deformations of the I/V curves are already evident at much shorter lifetimes.

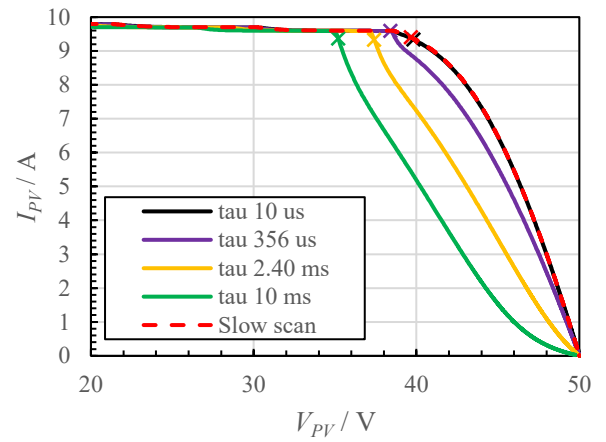


Figure 7: Effects of minority charge carrier lifetimes on the simulated I/V curves.

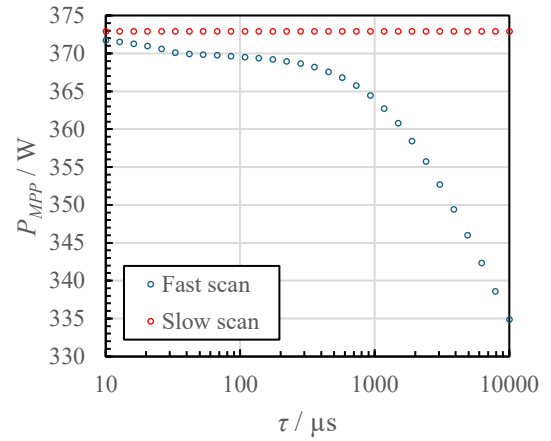


Figure 8: Effects of minority charge carrier lifetimes on the simulated P_{MPP} .

3.3 Mismatch factor MF

Inside the PV module all the HIGH cells have the same global short circuit current I_{SC} . The LOW solar cells in each PV substring, each have their own short circuit current, presented with a current source $I_{SC_MIN_X}$, where X is the number of PV substrings. Mismatch factor MF refers to percental difference between the lowest LOW cell ($I_{SC_MIN_4}$) and the HIGH cells (I_{SC}). Each substring has its own short circuit current calculated in accordance with the equations (1-4).

$$I_{SC_min_1} = I_{SC} \cdot \left(1 - \frac{MF}{100 \cdot 4}\right) \quad (1)$$

$$I_{SC_min_2} = I_{SC} \cdot \left(1 - \frac{MF}{100 \cdot 2}\right) \quad (2)$$

$$I_{SC_min_3} = I_{SC} \cdot \left(1 - \frac{MF \cdot 3}{100 \cdot 4}\right) \quad (3)$$

$$I_{SC_min_4} = I_{SC} \cdot \left(1 - \frac{MF}{100}\right) \quad (4)$$

MF besides the PV module capacitances plays a crucial role right around the P_{MPP} as is presented in figure 9. The threshold at which the uneven short circuit current starts conflicting with P_{MPP} is at around 1 %. The effect of MF on MPP is presented in figure 10.

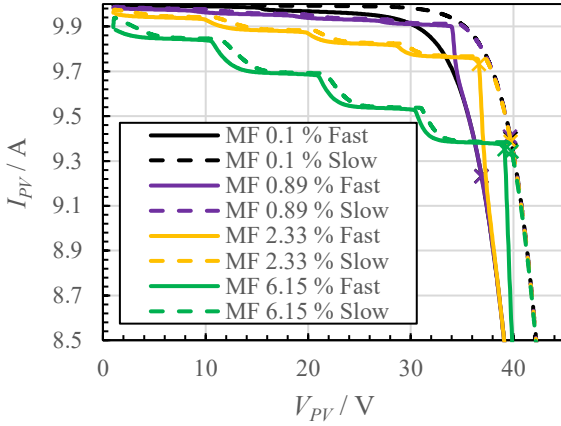


Figure 9: Effects of mismatch factor on the simulated IV curves.

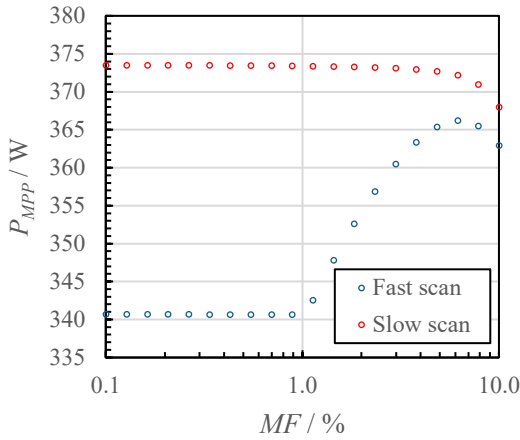


Figure 10: Effects of mismatch factor on the simulated P_{MPP} .

3.4 Reverse breakdown voltage V_{REV}

To simulate the reverse breakdown properties, we implemented reverse diode inside each LOW group of each PV substring. From the set voltage V_{REV} , diode ideality factor N_{REV} as well as reverse saturation current I_{SO_REV} are calculated according to equation 5. The bypass diode will conduct I_{SC} of current when exposed to the reverse voltage V_{REV} .

$$I_{SO_REV} = 1 \mu A \quad (5)$$

$$N_{REV} = \frac{V_{REV} \cdot q}{\ln\left(\frac{I_{SC}}{I_{SO_REV}} + 1\right) \cdot V_t}$$

The effect of reverse breakdown voltage on the IV curve is presented in figure 11. While the effects are visible in the region from I_{SC} towards P_{MPP} , the overall effect on the P_{MPP} presented in figure 12 is minimal.

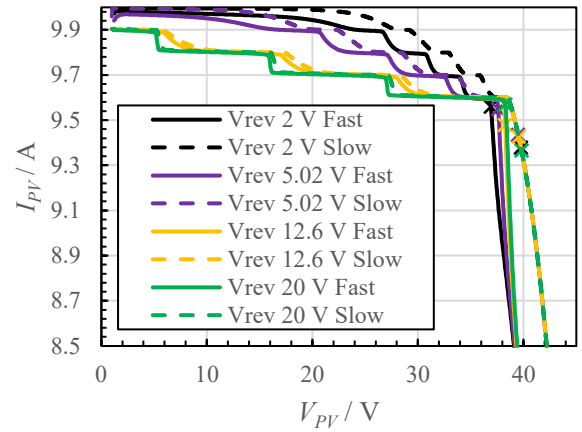


Figure 11: Effects of reverse breakdown voltages on the simulated IV curves.

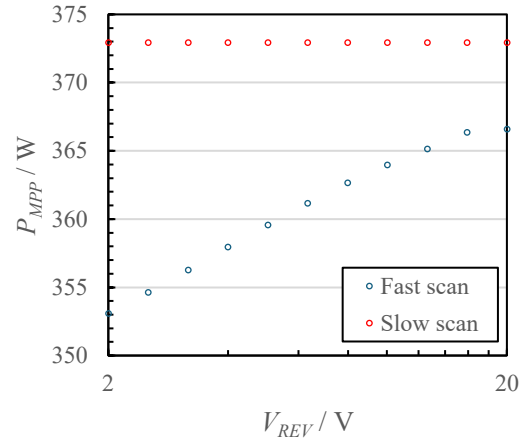


Figure 12: Effects of reverse breakdown voltage on the simulated P_{MPP} .

3.5 Uniformity of mismatch RHL

In real operating conditions we can have any ration between the number of LOW and HIGH cells. For this reason, we introduced Ratio Hight Low (RHL) factor, which can be converted into numbers of each cell type according to equations 6 and 7. The total number of cells inside each PV subsector always stays the

same. The same *RHL* is applied to all subsectors inside the PV module.

$$\text{Number HIGH cells} = RHL - 1 \quad (6)$$

$$\text{Number LOW cells} = 21 - RHL \quad (7)$$

From the simulations in figure 13 we can see that the *RHL* has a mild impact on the *IV* curve scans and the same can be observed on P_{MPP} , as is presented in figure 14.

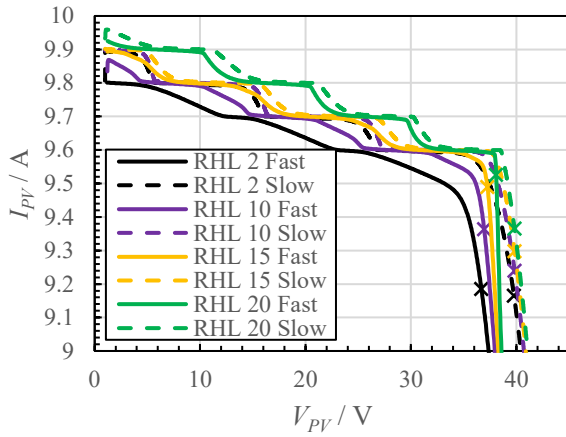


Figure 13: Effects of uniformity of mismatch on the simulated *IV* curves.

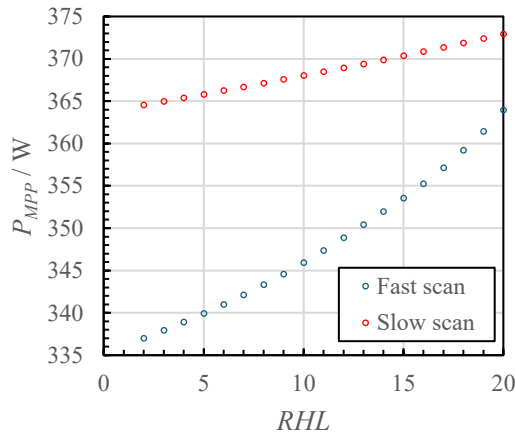


Figure 14: Effects of uniformity of mismatch on the simulated P_{MPP} .

4 Conclusion

In future work we will fit the measured *IV* curve scans of HE PV modules to simulation model presented. The sensitivity analysis presented in this paper should accelerate the process of finding the right set of parameters to achieve agreement. All five analyzed parameters affect the simulated PV modules' P_{MPP} . Notably, even slight short circuit current

differences between cells can cause substantial distortions of the simulated *IV* curve. Mismatches of this magnitude occur readily under outdoor conditions, which suggests the effect is relevant to the field measurements.

5 Acknowledgments

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Compositional Design of Wide-Bandgap Perovskites for Efficient and Stable Tandem Photovoltaics

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Abstract: This work investigates a compositional design strategy to develop wide bandgap perovskite absorbers for tandem integration. We explored a controlled variation of halide ratios (I/Br) in MA-free compositions to tune the perovskite bandgap toward ~1.75 eV while mitigating halide segregation under illumination. Additional fabrication routes, involving interface engineering and additive incorporation, are evaluated to suppress non-radiative recombination and improve long term stability. The use of 4PADCb as a self-assembled monolayer showed considerable electrical improvement on perovskite wide bandgap devices. On the other hand, the addition of DMAI significantly reduced phase segregation under continuous illumination, while increased the initial bandgap from 1.73 to 1.76 eV.

Keywords: perovskite; wide bandgap; stability; additive engineering;

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1 Introduction

Tandem solar cells overcome the theoretical limitation of single junction devices (~33%) by stacking two or more photovoltaic (PV) layers with complementary bandgaps, better utilizing solar spectrum while reducing losses. Wide bandgap metal-halide perovskites (1.70 - 1.80 eV) are essential for high efficiency tandem photovoltaics, yet their practical implementation remains limited mainly by phase instability, sub-optimal optoelectronic quality.[1-2]. Most of this loss originates at the bulk and at the interface with charge selective layers. Interface engineering, like the use of specific self-assembled monolayers (SAMs) or buffer layers, can help with the improvement of charge extraction and defect passivation.[3] Similarly, additive incorporation has a direct impact on defect passivation and film

morphology, leading to more stable phases.[4-5]

In this work, we analyze solar cell performance of 4 different perovskite bandgaps. To improve performance, we explore two different SAMs, MeO-2PACz and 4PADCb. To improve phase stability, we analyze the influence of Dimethylammonium iodide (DMAI) as an additive.

2 Materials and Methods

We prepared perovskite solutions at 1.1M with the stoichiometry $\text{FA}_x\text{Cs}_{1-x}\text{Pb}(\text{I}_y\text{Br}_{1-y})_3$, where $x=0.83$ and $y=0.17$ for reference devices. Y amount was then varied to tune the bandgap. Stock solutions were prepared at 1.35M by

dissolving PbI_2 , PbBr_2 in DMF:DMSO with a ratio of 4:1, while CsI was dissolved in DMSO. Stock solutions were then added to formamidinium iodide (FAI) with 5 mol% PbI_2 excess. DMAI was dissolved in DMF:DMSO 4:1 and added to the final solution in % excess as denoted in the text.

Inverted planar PSCs were prepared with the stack configuration: Glass/ITO/SAM/Perovskite/ C_{60} / SnO_2 /Cu. Glass substrates with a patterned ITO layer (for a final active area of 0.17 cm^2) were first washed and treated with UV-ozone for 15 minutes. Self-assembled monolayer (either MeO-2PACz or 4PADCB) dispersed in ethanol (0.1 mg/ml) was spin-coated for 30 s at 3000 rpm and annealed at 100°C for 10 minutes. Perovskite layer was deposited then via spin-coating at 4000 rpm for 35 s, adding ethyl acetate after 25 s of initiating the spin-coating process (perovskite films were also fabricated on glass substrates in the same batch for optical measurements). Samples were annealed for 40 min at 100°C . Then, 21 nm C_{60} was thermally evaporated at $0.1 \text{ \AA/s}$, followed by 20 nm SnO_2 deposited via ALD at 100°C using tetrakis(dimethylamino)tin(IV) (TDMASn) from as precursor and water as reactant. Cell was completed with 100 nm of copper, thermally evaporated at $1 \text{ \AA/s}$. Silver paint was used to improve electrical contact.

PV performance was determined from the I-V measurements taken under Newport (Xen-on lamp, class ABA) sun simulator with a Keithley 2400 source meter unit. Photoluminescence (PL) measurements were performed using LuQY Pro with 532nm laser and 1 sun intensity in single (average of 5 spectra) and continuous (spectra in a 1-hour lapse with 15 second separation between them) modes.

3 Results and discussion

3.1 Halide variation

We first varied the halide ratio to widen the perovskite bandgap. Initially, y was varied

between 0.83 (reference), 0.65, 0.60 and 0.55, resulting in bandgaps of 1.61 eV, 1.69 eV, 1.73 eV and 1.75 eV, respectively, as extracted from photoluminescence measurements. (table 1)

Phase stability of perovskite films was optically analyzed using PL measurements (see Fig 1a). Under light, perovskite absorbers with mixed halides segregate into regions richer with iodide and those richer with bromide. The former dominates, reducing the perovskite bandgap, exhibited as a peak increase around 780 nm. In the case of the reference composition, the difference is negligible as the initial and final bandgap are the same after 1 hour of continuous illumination (table 1). With increased bandgap, the phase segregation occurs sooner and is stronger, resulting in lower final bandgap, as it clearly seen on the insets of figure 1a. This can be interpreted as lower stability of wider bandgaps.

Table 1: Initial and final bandgap from continuous PL measurements varying halide composition. PL single measurements. were taken right after fabrication.

Halide	PL (single)	Initial E_g	Final E_g
$y=0.83$	1.61	1.61	1.61
$y=0.65$	1.69	1.71	1.66
$y=0.60$	1.73	1.74	1.59
$y=0.55$	1.75	1.75	1.59

The electrical performance of such compositions is shown in figure 1b. There is a clear trend dependent on the bandgap, where PCE, J_{sc} and FF decrease as the bandgap increases, while voltage increases. The use of 4PADCB as charge selective layer considerably improved the electrical performance compared to the reference SAM (MeO-2PACz), while keeping the same trend. For instance, for the widest bandgap the PCE increases by 2%, due to improvement in open circuit voltage (1.2 V vs. 1.14 V for MeO-2PACz) and the current density (3 mA/cm^2).

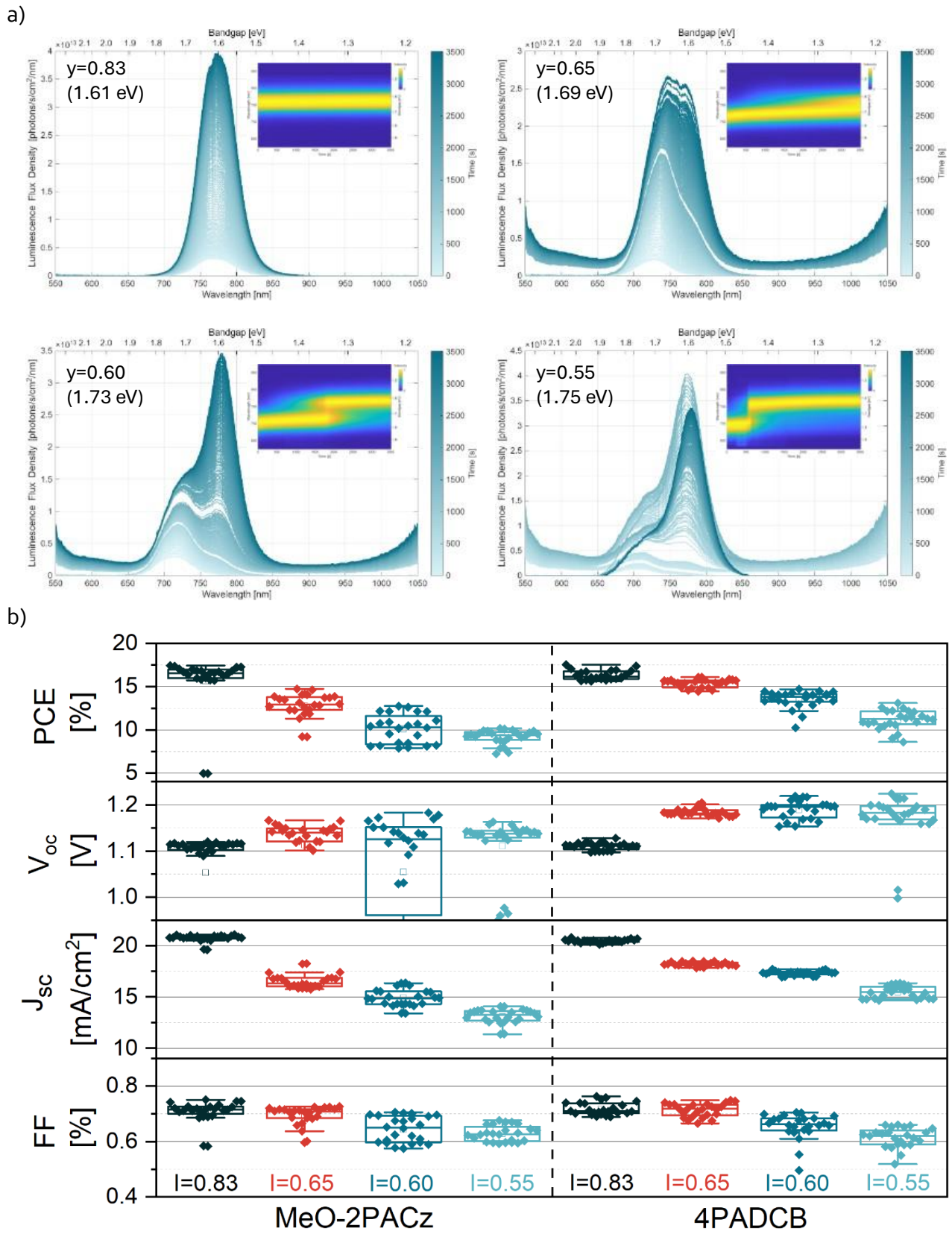


Figure 1: a) Continuous PL measurements of perovskite films. b) Electrical parameters of PSC devices with MeO-2PACz and 4PADCz as SAM, in function of halide compositions.

3.2 DMAI additive

Considering the beneficial impact of ${}_{4}\text{PADCBC}$ on electrical performance, we selected this SAM to be used with perovskite $y=0.60$, as a midpoint between stability and electrical performance. We added DMAI as an additive with 4, 8, and 12 molar% to see the impact on stability. As seen in figure 2, the addition of DMAI drastically impacts the electrical performance, lowering the PCE down to 5%. All PV performance parameters are considerably lower than in the reference sample without DMAI ($y=0.60$) and performance drops with the higher concentration of the additive. On the other hand, Figure 3 shows an improvement in phase stability when adding DMAI, as measured by continuous PL. In contrast to figure 1, perovskite films with DMAI show a smooth transition to lower energies, shifting the bandgap rather than the abrupt appearance of the peak at 780 nm. Moreover, the final bandgap they reach after almost an

hour of constant light stops around 1.65. (see table 2), 50 meV higher than the reference.

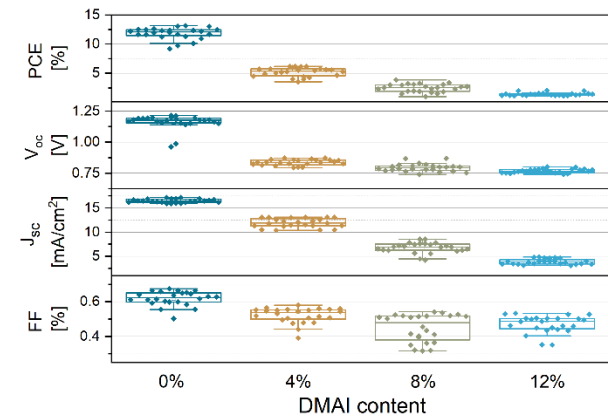


Figure 2: Electrical parameters of PSC devices with DMAI as an additive.

Table 2: Initial and final bandgap from continuous PL measurements in function of DMAI concentration. PL single measurements were taken right after fabrication.

DMAI %	PL (single)	Initial E_g	Final E_g
0%	1.73	1.75	1.59
4%	1.74	1.74	1.63
8%	1.74	1.75	1.66
12%	1.76	1.76	1.67

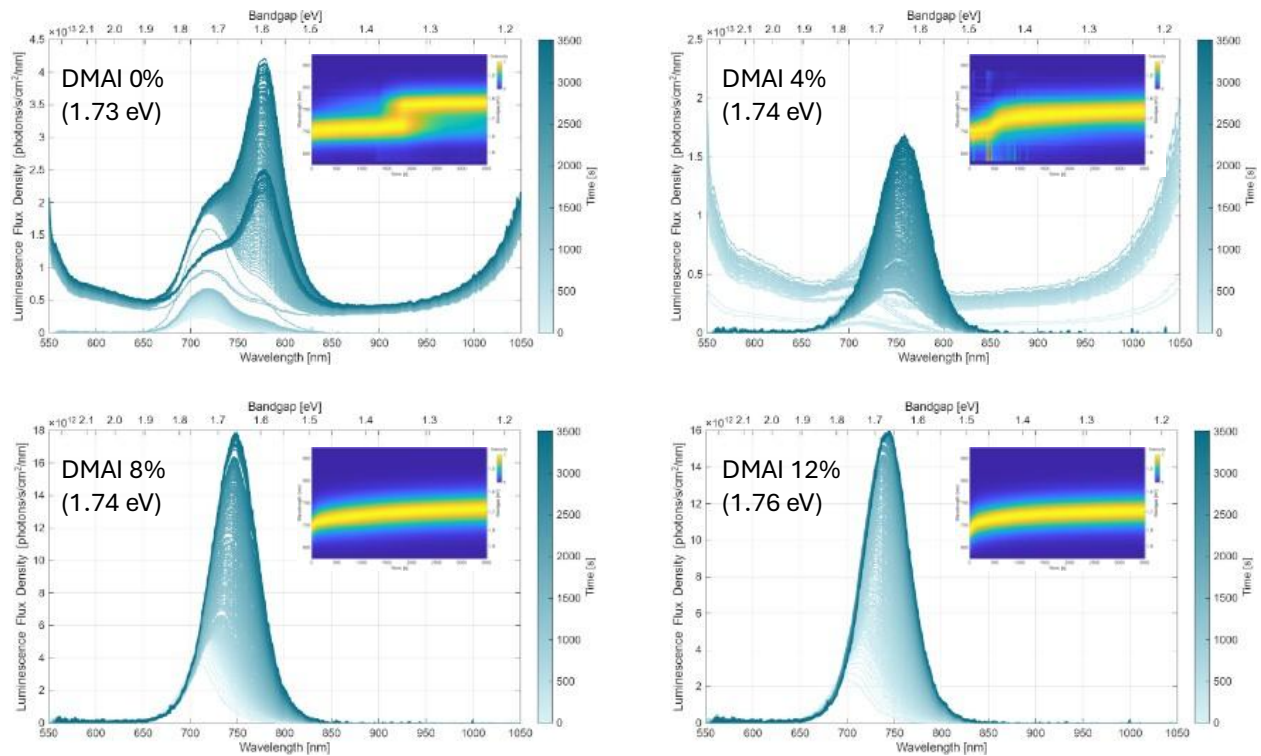


Figure 3: Continuous PL measurements of perovskite films with DMAI at different concentrations. Stoichiometry of $y=0.60$ for the perovskite films.

4 Conclusions

We explored different perovskite compositions by tuning the halide ratio. Using I:Br ratios of 0.65:0.35, 0.60:0.40 and 0.55:0.45, bandgaps were successfully increased from 1.61 eV to 1.69 eV, 1.73 eV and 1.75 eV, respectively. However, the electrical performance and stability were compromised with an increase in Br content. Changing MeO-2PACz SAM with 4PADCz resulted in improvement in electrical performance. The addition of DMAI to the perovskite precursor indicates a huge improvement in phase stability, although the electrical performance is considerably affected. Future research may be targeted to tune these components to reach higher stability without affecting their performance.

5 Acknowledgements

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INTEGRATED CIRCUITS AND ELECTRONICS

A Switched-Capacitor Auto-Zeroing Ripple Reduction Loop for a Low-Noise Chopper Charge Amplifier used in an Artificial Nose detection system

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Abstract: Developing precision amplifiers for detecting small charge variations is crucial for advanced sensor applications, particularly in Artificial Nose (ANose) detection systems [1–8]. The ANose relies on detecting extremely small differential capacitance changes, caused by target molecule adsorption, to identify complex chemical compounds. While previous system iterations successfully integrated 30 differential capacitive sensor pairs, scaling the next-generation architecture to 256 pairs on a single ASIC demands an extremely low-noise input charge amplifier. To meet these requirements, a fully differential, chopped amplifier design is utilized. However, chopping techniques inherently introduce unwanted output ripples. This work presents a detailed analysis of a switched-capacitor Auto-Zeroing (AZ) amplifier that serves as the core of a Ripple Reduction Loop (RRL), specifically designed to suppress these artifacts. The scientific innovation lies in this advanced switched-capacitor architecture and the specific ripple reduction mechanism, which will be presented in detail. The AZ amplifier operates in two distinct phases: in the first phase, the circuit is configured to eliminate its own internal offset voltage, while in the second phase, it detects the offset voltage of the primary chopped amplifier, which is then processed by a transconductance amplifier to subtract the corresponding error from the current in the first-stage PMOS folded cascode. Preliminary results indicate that integrating this AZ-based RRL allows the central system to process small charge transfers without the interference of static errors or chopping ripples, thereby significantly increasing the dynamic range and absolute accuracy, and proving essential for achieving the strict low-noise performance required for the 256-channel ANose ASIC.

Keywords: *switched-capacitor*; auto-zeroing, ripple reduction loop, charge amplifier, artificial nose

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1 Introduction

Noise optimization and reduction play a critical role in measuring extremely small signals, requiring amplifier topologies optimized for low-noise performance. Over the past decade, significant effort has been devoted to offset and $1/f$ noise compensation techniques. For instance, Fan et al. [1] presented a

low-power capacitively coupled chopper instrumentation amplifier (CCIA) utilizing a positive feedback loop and a ripple reduction loop (RRL). Similarly, a fill-in technique was proposed in [2] to suppress chopper-induced intermodulation distortion (IMD) by approximately 28 dB, while a dynamic offset zeroing

(DOZ) method in [3] mitigates chopping ripples by 61 dB.

Compared to prior CCIA designs, our work pushes sensitivity to a new regime (zepto-farad-level detection) through full noise analysis and a fully differential architecture suitable for large-scale sensor arrays. The main purpose of our artificial nose (ANose) detection system is to mimic the biological olfactory mechanism by transitioning from an earlier design with 30 separate ASICs [4, 5, 6, 7, 8, 9] to a next-generation platform integrating 256 capacitive sensor pairs on a single ASIC. Because front-end electronics are crucial for sensitivity, this study focuses on optimizing a single channel of the ANose system through careful noise analysis and a switched-capacitor auto-zeroing ripple reduction loop. In this paper, we will focus particularly on the auto-zeroing principle of operation within the RRL.

The rest of this paper is organized as follows. Section II describes the one channel of the ANose System. Section III describes the ripple reduction loop (RRL), section IV describes switched-capacitor auto-zeroing amplifier and its integration into the ripple reduction loop (RRL), followed by the simulation results. Finally, Section VI concludes the paper.

2 One Channel of the ANose System

The sensitivity of the proposed ANose lies in the zeptofarad (zF) range, demanding an exceptionally high signal-to-noise ratio (SNR) of the charge amplifier, which is the most important part of ANose in terms of sensitivity. It is challenging to achieve such performances in 180 nm CMOS technology, with its relatively high intrinsic flicker noise and input offset voltage. To overcome these limitations, a fully differential chopper charge amplifier was developed, that accommodates the connection of a fully differential capacitive sensor pair.

Amplifiers with chopping shifts the sensor signal away from the low-frequency noise band, amplifies the whole spectrum, transforms charges to voltage, and suppress the remains of the $1/f$ noise and offset voltage. Fig. 1 presents a simplified circuit diagram of a fully differential charge amplifier in each channel of the ANose, which consists of several essential building blocks required for accurate low-noise signal acquisition. A programmable DC input source generates two reference voltages, V_{sp} and V_{sn} , that form the differential excitation of the sensor. These voltages are modulated by the input differential choppers Ch01, producing square-wave signals V_{in1} and V_{in2} with a programmable chopping frequency. Modulated excitation is applied to a pair of differential capacitive sensors, as illustrated in Fig. 1.

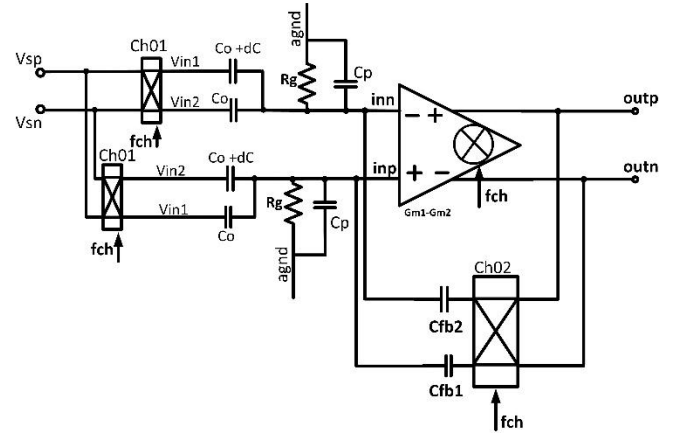


Figure 1: Fully differential charge amplifier.

3 Ripple reduction loop (RRL)

The ripple appears at the output of the transconductance amplifier owing to the up-modulated offset and $1/f$ noise. Several effective techniques for ripple mitigation, including filtering and ripple suppression, have been reported in the literature [2, 3]. A widely used approach to reduce this effect is the ripple-reduction loop (RRL), the simplified schematics of which are shown in Fig. 2.

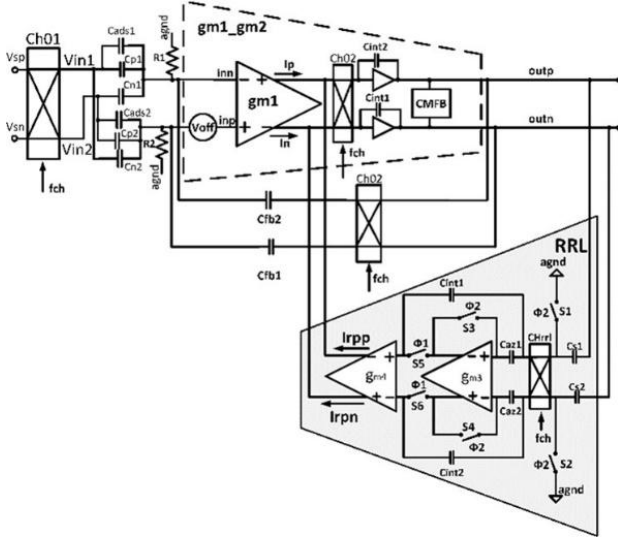


Figure 2: Fully differential charged chopper amplifier with RRL.

The RRL was specifically designed to detect the ripple at the amplifier output. Once the ripple is detected, the RRL generates compensating currents I_{rpp} and I_{rpn} to counteract the low-frequency current produced by the offset voltage and the $1/f$ noise voltage of the transconductance stage $Gm1$. Ideally, this approach can completely suppress the ripple; thus, the output ripples at V_{outp} and V_{outn} should theoretically vanish when the RRL is active [1]. The ripple caused by the offset voltage could be reduced by decreasing $Gm1$ or increasing C_{int} . However, reducing $gm1$ increases system noise, making this approach impractical. Varying the chopping frequency f_{ch} and the integration capacitance C_{int} affects the residual offset, chip area, and power consumption. By employing RRL, the system effectively suppresses the output ripple and consequently improves the overall performance of the charge amplifier.

The ripple voltage at the output can be expressed by equation (1):

$$V_{ripple} = \frac{V_{offset} gm1}{2f_{chop} C_{int}} \quad (1)$$

The block diagram and main components of the RRL are shown in Fig. 2. This architecture

illustrates the structure of the RRL and highlights the core functional blocks responsible for the ripple suppression. The RRL comprises the following key components:

- **Sensing capacitors ($C_{S1,2}$):** These capacitors sense a large ripple voltage at the amplifier output and convert it into an AC current proportional to the ripple slope.
- **Demodulating chopper (CH_{rrl}):** This block demodulates the AC current generated by the sensing capacitors, isolating the ripple component for further processing.
- **Integrator:** The integrator processes the demodulated signal, acting as a low-pass filter, and converts the AC current into a voltage proportional to the ripple amplitude. It also functions as a sample-and-hold (S/H) stage.
- **Compensation transconductor (gm_4):** Based on the integrated ripple signal, gm_4 generates compensating currents to cancel the ripple-induced output disturbance.

The RRL generates a notch at the chopping frequency f_{ch} , with the bandwidth determined by design parameters such as $C_{S1,2}$ and gm_4 [1]. A passive integrator implemented with a current buffer and an integration capacitor exhibits an offset originating from the buffer, producing a second-harmonic ripple. This effect typically requires large integration capacitors for adequate suppression [1, 2, 3]. To address this, a switched-capacitor (SC) integrator with automatic zeroing was employed (see Fig. 2).

4 Auto-Zeroing Operation Principle in Switched-Capacitor Integrator

The integrator offset is stored in auto-zero capacitors ($C_{az1,2}$) during one clock phase. The

self-zeroing SC integrator periodically samples and cancels the offset voltage, reducing the error in both the integrator and S/H stage. A key design constraint is that the output of the integrator must be stable during the auto-zero storage phase; otherwise, unwanted compensation currents may be injected into the main amplifier (block G_{m1} & G_{m2}). During this phase, the voltage at the input of gm_4 is held constant by the charge stored on C_{int1} and C_{int2} .

The SC integrator consists of sampling capacitors $C_{s1,2}$, a demodulating chopper CH_{rrl} , integration capacitors $C_{int1,2}$, autozero capacitors $C_{az1,2}$, and a single-stage OTA gm_3 . The demodulation chopper is clocked at f_{ch} , whereas switches S_1 – S_6 operate at the auto-zero frequency $f_{az} = f_{ch}/2$. The signal f_{az} includes the integration phase ϕ_1 and auto-zero phase ϕ_2 , each spanning a complete cycle of the chopping frequency. The full-cycle RRL operation during ϕ_1 allows for accurate ripple detection and storage. During ϕ_1 , $C_{s1,2}$ converts the ripple voltage into current. After demodulation, this current was integrated into C_{int1} and C_{int2} . The resulting voltages drive gm_4 , producing differential compensation currents that cancel the offset introduced by gm_1 . During ϕ_2 , the sensing capacitors are shorted to the analog ground, preventing ripple-current integration. Meanwhile, the previous C_{int} voltages were held constant and continued to bias gm_4 . In this configuration, no additional ripple is introduced during ϕ_2 , and the input of gm_4 remains stable. The OTA gm_3 is configured for unity gain, allowing its offset to be sampled and stored in $C_{az1,2}$. Throughout ϕ_2 , the integration capacitors remain isolated from gm_3 , hold the voltage from the prior ϕ_1 , and continue to drive gm_4 .

During the integration phase ϕ_1 , the RRL actively detects and processes the output ripple voltage of the primary charge amplifier:

- **Ripple-to-Current Conversion:** Sensing capacitors ($C_{s1,2}$) convert the large

ripple voltage present at the amplifier output into an AC current proportional to the ripple slope.

- **Demodulation and Integration:** The demodulation chopper (CH_{rrl}), clocked synchronously at f_{ch} , demodulates this AC current. The resulting signal is integrated by the integration capacitors ($C_{int1,2}$) connected across the OTA (gm_3).
- **Compensation Current Generation:** The integrated voltage across $C_{int1,2}$ drives the compensation transconductor (gm_4), which in turn injects differential compensation currents (I_{rpp} and I_{rpn}) into the main amplifier stage (G_{m1} – G_{m2}). This cancels the low-frequency offset and ripple components.
- Simultaneously, the OTA's internal offset is effectively managed, ensuring that true ripple suppression takes place continuously throughout ϕ_1 .

During the auto-zero phase ϕ_2 , the circuit transitions to a self-calibration and holding state to suppress intrinsic errors of the SC integrator itself:

- **Isolation of Sensing Path:** The sensing capacitors ($C_{s1,2}$) are shorted to the analog ground, safely halting any further ripple-current integration and preventing the injection of switching transients.
- **Offset Storage (Auto-Zeroing):** The OTA (gm_3) is temporarily configured in a unity-gain feedback configuration. In this state, its input offset voltage is sampled and stored onto the dedicated auto-zero capacitors ($C_{az1,2}$). This periodic sampling effectively neutralizes the OTA's DC offset and eliminates low-frequency drift.
- **Voltage Retention:** While the OTA is undergoing auto-calibration, the integration capacitors ($C_{int1,2}$) remain completely isolated from gm_3 . They

maintain and hold the exact differential voltage level established during the preceding ϕ_1 phase.

- **Continuous Bias Stability:** Because the charge on $C_{int1,2}$ is preserved, the bias voltage applied to the input of the compensation transconductor (gm_4) remains constant. Consequently, continuous ripple compensation is sustained without interruption or the introduction of secondary disturbance artifacts during ϕ_2 .

5 Results

By alternating between ϕ_1 and ϕ_2 , the switched-capacitor auto-zeroing RRL successfully decouples continuous ripple suppression from amplifier offset. This synergy enables the system to suppress output ripple voltages by approximately two orders of magnitude (as demonstrated in the simulation results), ensuring the ultra-low-noise performance required for the 256-channel ANose.

Fig. 3 shows the output of the differential charge amplifier when dC is set to 0. The measured ripple when the RRL is off is 0.02608 V. Simulated measured result when the RRL is on is presented in Fig. 4. Simulation results show that with the adsorption capacitance $dC = 0$ and the RRL enabled, the output ripple voltage is reduced to 0.00038. As summarized in Table I, the RRL suppresses the unwanted ripple by approximately two orders of magnitude.

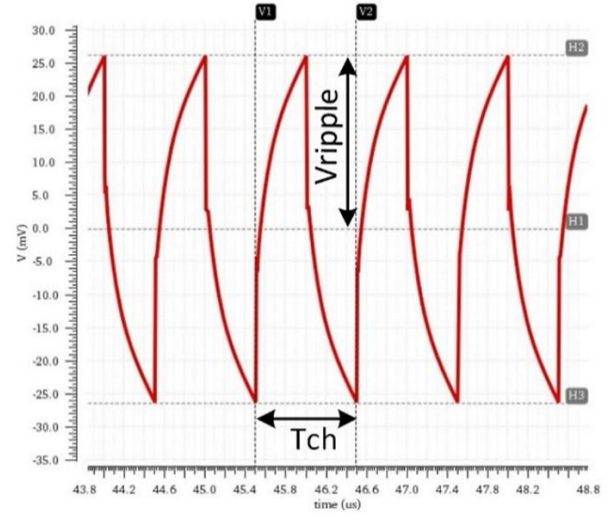


Figure 3: Simulated output ripple of the fully differential charge amplifier operating without RRL. Tch is the chopping period and Vripple represents output ripple voltage in Tch/2.

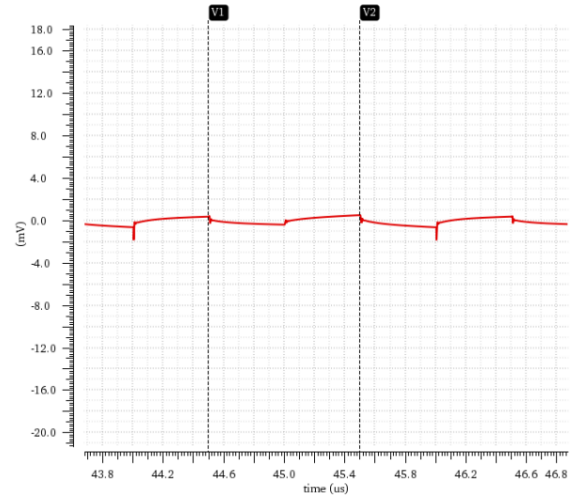


Figure 4: Simulated output ripple of the fully differential charge chopper amplifier operating with RRL.

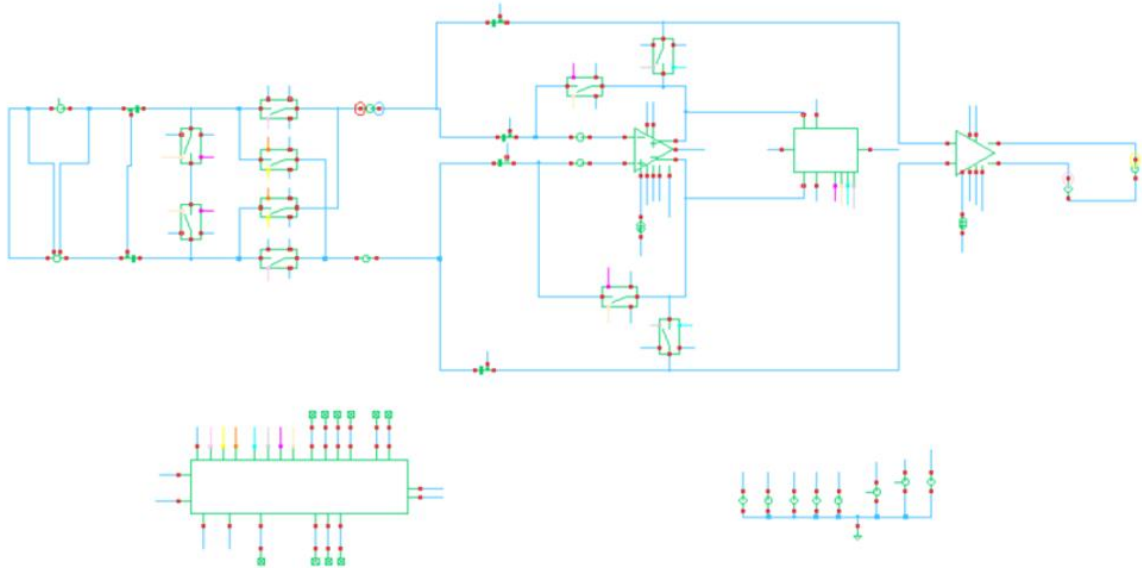


Figure 5: Block diagram of the RRL with AZ OTA and transconductance amplifier.RRL.

Table 1: Different values of C_{ads} without and with RRL.

	C_{ads}	RRL	V_{ripple}
1.	0fF	No	0.02608 V
2.	100fF	No	0.02634 V
3.	0fF	Yes	0.00038 V
4.	100fF	Yes	0.0003 V

6 Conclusions

This paper presented a fully differential chopper charge amplifier featuring a switched-capacitor auto-zeroing ripple reduction loop (RRL), specifically designed for the high-precision 256-channel Artificial Nose (ANose) ASIC. By integrating a switched-capacitor integrator with an auto-zeroing scheme operating at $f_{az} = f_{ch}/2$, the proposed architecture successfully decouples continuous ripple suppression from amplifier offset calibration, eliminating second-harmonic ripples without introducing switching transients or requiring excessively large integration capacitors.

Simulation and measurement results demonstrate that the RRL effectively suppresses unwanted output ripples by approximately two orders of magnitude, reducing the ripple voltage from 0.02608 V down to 0.00038 V at

zero adsorption capacitance ($C_{ads} = 0$ fF). Furthermore, the system maintains robust ripple attenuation across varying sensor input conditions, such as $C_{ads} = 100$ fF. These achievements confirm that the proposed switched-capacitor auto-zeroing RRL provides the required zeptofarad-level sensitivity, high signal-to-noise ratio, and ultra-low-noise performance essential for scalable, high-precision chemical sensing applications.

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Transient Noise Simulation in VACASK

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Noise is a fundamental concern in analog and RF circuit design. While small-signal AC noise analysis, as implemented in most SPICE-derived simulators, provides useful spectral information around a linear time-invariant operating point, it cannot capture the behavior of circuits where noise interacts with large-signal nonlinear dynamics. Oscillators, phase-locked loops, mixers, and sampling circuits are canonical examples. The correct framework for these cases is transient noise simulation, in which device noise sources are represented in the time domain and injected directly into the circuit equations.

VACASK (the Verilog-A Circuit Analysis Kernel) [1] is a free and open source analog circuit simulator that uses the OpenVAF Verilog-A compiler [2] and the OSDI (Open Source Device Interface) to load compact device models as shared libraries at runtime. This architecture provides a clean separation between device model equations and simulation algorithms, which is particularly advantageous for implementing new types of circuit analysis, such as transient noise. The noise source contributions declared inside a Verilog-A model via the standard `white_noise()` and `flicker_noise()` built-in functions are directly accessible to the simulator through the OSDI API, without any modification to the model code. VACASK exploits this to implement fully automatic, device-level transient noise analysis, believed to be a first among FOSS circuit simulators. Every device in the circuit, whether a resistor, diode, or transistor described by a modern compact model such as PSP or BSIMBULK, automatically contributes its own noise during a transient run, in the same manner as in commercial RF simulators such as Spectre.

VACASK implements two distinct and complementary approaches to transient noise, which differ in how the stochastic noise sources are discretized and coupled to the time-domain solver.

The first is the zero-order hold (ZOH) approach. [3] Here, a user-specified noise bandwidth $F_{\max}$ defines a noise update interval $T_n = 1/(2F_{\max})$. At each noise update, independent Gaussian noise current samples with zero mean and variance $S/(2T_n)$ are drawn for every white noise source in every device, and these samples are held constant at their drawn value until the next update. The circuit simulation timestep is constrained to T_n . Flicker ($1/f$) noise is handled by approximating the $1/f$ power spectral density as a sum of first-order Lorentzian shaping filters driven by independent white noise sources, with pole frequencies logarithmically distributed across the frequency range of interest. The ZOH method is straightforward to implement, produces noise sources with a well-defined and user-controlled bandwidth, and integrates cleanly with a standard Newton-Raphson transient solver.

The second is the stochastic differential-algebraic equation (SDAE) approach. [4] In this formulation, the ordinary DAE system of transient analysis is extended to an SDAE by adding stochastic terms directly to the current balance equations. White noise sources are modeled as increments of a Wiener process: over a timestep h , a white noise source with one-sided spectral density S contributes a random current drawn from a Gaussian distribution with zero mean and variance $S/(2h)$, so that the injected noise automatically scales with the actual simulation timestep rather than a separately specified bandwidth. This is the key distinction from the ZOH approach: the noise bandwidth is implicitly determined by the adaptive stepsize chosen by the solver. The standard



implicit integration scheme is used as the integrator. Flicker noise in the SDAE framework is handled via the same shaping filter bank as in the ZOH approach, but with the filter states now evolving as additional stochastic state variables. Due to the filter's simplicity, we can use an exact update formula for computing the injected flicker noise current.

The implementation is tested on several small test circuits as well as an LC oscillator. The latter example demonstrates the extraction of the phase noise and phase jitter from simulation results. Planned future developments include (quasi)periodic noise analysis based on harmonic balance and periodic steady-state analyses.

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A Grammatical-Evolution-Based Front-End for Automated EEC Initialization in EIS

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1 Abstract

Electrochemical Impedance Spectroscopy (EIS) is widely used for characterization of electrochemical systems through Equivalent Electrical Circuit (EEC) modelling. However, accurate fitting of EEC models typically depends on expert-driven selection of circuit topology and careful initialization of model parameters prior to local optimization using algorithms such as the Levenberg-Marquardt Algorithm (LMA). This process remains time-consuming, subjective, and difficult to automate.

This work presents a novel automated front-end for EIS analysis based on Grammatical Evolution (GE) integrated with the SPICE circuit simulation environment. The proposed approach automatically synthesizes candidate EEC topologies while simultaneously generating initial parameter estimates suitable for subsequent local optimization. To support realistic EIS modelling within SPICE, Constant Phase Element (CPE) and ZARC elements were implemented using the XSPICE framework and integrated into the simulation workflow through PyOPUS.

The GE framework uses grammar-defined topology blocks and evolutionary operators to explore the EEC search space and evaluate generated models using the Sheppard criterion. Validation was performed on synthetic ZARC datasets with and without added Gaussian noise. Experimental results demonstrate that the proposed method successfully identifies appropriate EEC structures and generates parameter estimates close to the original values used for synthetic data generation.

The presented framework represents an important step toward automated and reproducible EIS analysis by reducing dependence on manual EEC initialization and expert intervention. The proposed front-end also establishes a foundation for future hybrid workflows combining evolutionary topology synthesis with gradient-based parameter refinement.

2 Introduction

EIS is widely used for characterization of electrochemical systems such as batteries, fuel cells, corrosion systems, and electrochemical materials. Interpretation of EIS measurements is commonly performed using EEC models, where measured impedance spectra are fitted to electrically equivalent topologies composed of resistors, capacitors, CPE, and distributed elements such as ZARC.

A major limitation of existing EIS fitting workflows is the strong dependence on expert knowledge during the selection of appropriate EEC topologies and initialization of model parameters. Gradient-based optimization methods, such as the LMA, are effective for local parameter refinement but require suitable initial conditions to ensure stable convergence.

This work proposes a Grammatical Evolution based automated front-end for EIS analysis that automatically synthesizes candidate EEC topologies and generates initial parameter estimates suitable for subsequent local optimization.

3 2. Methodology

The proposed framework combines Grammatical Evolution, SPICE circuit simulation, custom EIS circuit elements, and fitness-based evolutionary optimization.

The workflow begins with random generation of candidate EEC structures using grammar-defined topology rules. Generated circuits are translated into SPICE netlists and evaluated through AC simulation using Spice Opus and the PyOPUS interface.

To support realistic EIS modelling inside the SPICE environment, CPE and ZARC elements were implemented using the XSPICE extension framework. This enables direct simulation of EIS-specific circuit behavior without mathematical approximations outside the simulator.

Generated EEC models are evaluated against synthetic impedance datasets using the Sheppard criterion, while the evolutionary process iteratively improves the population through selection, crossover, mutation, and elite preservation.

4 3. Experimental Validation

Validation was performed using synthetic ZARC datasets generated with known parameters over the frequency range from 0.01 Hz to 100 kHz. Additional Gaussian noise was introduced to simulate experimental conditions.

The proposed method successfully identified suitable EEC topologies, generated stable initial parameter estimates, and maintained robust performance under noisy conditions. The generated EEC structures closely matched the mathematical form of the original synthetic models, while extracted parameter values remained close to the reference values used during dataset generation.

5 4. Conclusion

The presented framework demonstrates that GE combined with SPICE simulation can serve as an effective automated front-end for EIS analysis. The proposed approach reduces reliance on manual topology selection and parameter initialization while generating suitable starting points for subsequent gradient-based optimization methods such as LMA.

Future work will focus on validation using experimental EIS datasets, expansion of the grammar with additional EIS elements, and integration with local optimization pipelines for fully automated hybrid fitting workflows.

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ABSTRACT



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A Single-Microcontroller Control System for Throttleable Rocket Engines

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Abstract: The precise regulation of thrust through liquid propellant engine throttling is a foundational requirement for advanced aerospace operations. While modern control architectures frequently rely on distributed networks to manage computational loads, this approach introduces significant physical and financial overhead. Legacy single microcontroller architectures suffer from processing latency caused by synchronous peripheral polling. To circumvent these limitations, this study proposes a consolidated Full Authority Digital Engine Control (FADEC) architecture utilizing a single microcontroller optimized for asynchronous Direct Memory Access (DMA). To evaluate performance, the proposed DMA architecture and a legacy dual microcontroller polling system were subjected to identical simulated operational loads using a Python test bench that injected communication packets at strict 200 ms intervals. Performance indicates that the DMA framework reduces the average loop execution time from approximately 190 ms to 2.2 ms. Furthermore, the modernized architecture eliminates a 15.22% packet loss rate observed in the legacy system and reduces active processor wait time from 11% to 0%. Although the asynchronous memory updating introduces execution jitter and a slight timestamp ambiguity during sensor data acquisition, the calculated worst case response cycle remains under 7 ms. This reduction in response time demonstrates that the time variance introduced by DMA is an acceptable engineering tradeoff, yielding a highly responsive, reduced complexity hardware foundation for active fluid management and critical fault reaction in rocket engines.

Keywords: rocket engine controller; throttling; polling; DMA

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1 Introduction

The precise regulation of thrust through liquid propellant engine throttling remains a requirement for advanced aerospace operations, enabling maneuvers such as propulsive landings, orbital rendezvous, and dynamic trajectory adjustments. Early chemical rockets developed in the 1930s were heavily constrained by their reliance on purely manual, mechanical control architectures [1]. As aerospace engineering progressed into the 1960s, the introduction of localized computing facilitated rudimentary onboard engine throttling and automated shutdown sequences. However, these systems were characterized by prohibitive size, high power consumption, and severe mass penalties, restricting their application to large scale launch vehicles [1]. Today, the demand for precise thrust vectoring and dynamic power regulation has driven the aerospace industry toward highly sophisticated digital control systems, where split second decision making is essential for mission success.

Contemporary aerospace propulsion relies predominantly on Full Authority Digital Engine Control (FADEC) architectures to manage engine behavior, removing mechanical linkages in favor of comprehensive

electronic control. High-performance commercial applications, such as the Rolls Royce Pearl aircraft engine family, utilize advanced FADECs to achieve optimal fuel metering, real time telemetry streaming, and automated fault diagnosis [2]. To handle the computational burden of these tasks while maintaining necessary redundancy, modern aerospace systems frequently employ distributed network architectures. While distributed processing successfully decentralizes low level functions across multiple smart nodes, it inherently necessitates complex interconnectivity, heavy wiring harnesses, and extensive bus arbitration. Consequently, this multi subsystem hardware approach significantly increases total system mass, physical footprint, and financial cost [2]. In the context of modern commercial spaceflight and academic aerospace engineering, where miniaturization and hardware consolidation are paramount, the physical and computational overhead of distributed FADEC systems represents a substantial developmental bottleneck that must be overcome.

To circumvent the weight and cost penalties associated with distributed networks, consolidating control

algorithms into a single microcontroller unit (MCU) presents a desirable alternative. However, legacy single MCU architectures have historically struggled to meet the stringent processing latency requirements of aerospace applications. Previous iterative designs, such as the legacy FADEC v5 architecture previously presented in our research [3], relied on an ATmega328P and an STM32 MCU. This older system utilized synchronous polling methods for sensor data acquisition and peripheral communication. In a polling driven architecture, the processor must continuously check peripheral status registers, resulting in blocking operations that needlessly consume valuable CPU clock cycles. In hard real time environments, this computational overhead prevents the main loop code execution from remaining strictly deterministic, introducing significant jitter and delaying critical actuation commands. For a throttleable liquid rocket engine, where the quick and precise timing of valve actuations dictates fuel to oxidizer mixture ratios and overall combustion stability, unpredictable valve behavior due to polling latency is unacceptable.

To address these inefficiencies and contribute to the ongoing miniaturization of aerospace control hardware [4], this paper proposes a consolidated, reduced complexity FADEC architecture. The primary objective of this research is to resolve the engine throttling control challenge while ensuring determinable actuator behavior without relying on a distributed network of processors. By transitioning away from legacy polling methods and proposing an architecture optimized for asynchronous multiprocessing on a single MCU, the system aims to eliminate the blocking latency that plagues traditional control algorithms. This framework integrates modernized electronic control for throttleable valves alongside established emergency shutdown mechanisms [3]. By outlining a unified system capable of handling both critical safety functions and dynamic thrust regulation simultaneously, this research seeks to demonstrate that complex fluid management does not require the heavy computational overhead of multi node systems.

2 Materials and Methods

2.1 Technical Implementation

The technical evolution from the legacy FADEC v5 to the proposed FADEC v6 architecture centers on the transition from a distributed, synchronous polling model to a consolidated, asynchronous Direct Memory Access (DMA) framework. The older v5 iteration relied on a dual microcontroller setup, utilizing both an STM32G431RBT6 and an ATmega328P, where the continuous polling of peripheral registers between the two processors introduced significant blocking latency. This computational overhead severely degraded the deterministic execution required for high-speed fluid management. The new v6 system eliminates this bottleneck by operating entirely on a single STM32G431 microcontroller utilizing DMA. This consolidated approach allows for

continuous background telemetry acquisition and communication without interrupting main CPU execution. This architectural shift is fundamentally what enables the precise throttling of the liquid rocket engine. By eliminating processor stalling, the single MCU system can predictably compute target actuator positions and drive the proportional ball valves in real time. This prevents the erratic mixing ratios and actuation delays associated with the legacy system's distributed processing, ensuring smooth, uninterrupted engine throttling.

To physically facilitate this dynamic throttling alongside emergency shutdown capabilities, with the valve schematic being presented in Figure 1, the hardware layer underwent a redesign to handle demanding operational loads. Both the legacy and proposed systems operate on a standard 24 V supply voltage, however, the older dual MCU v5 hardware was severely constrained by thermal and current limitations, typically experiencing failure when sustained loads exceeded 5 A. In contrast, the modernized v6 power stage is rated to handle up to 90 A, providing thermal headroom and reliability for high torque valve actuation.

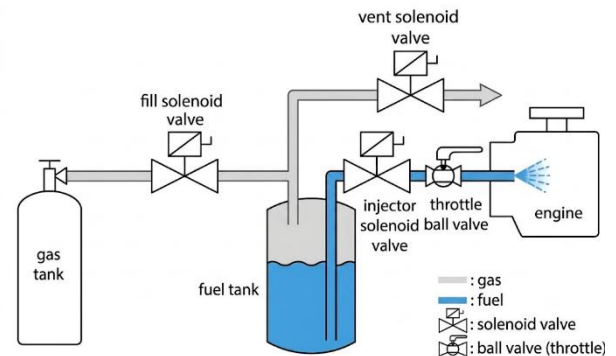


Figure 1: New engine line setup to enable throttling capabilities

Both versions of the system share the same solenoid valve actuation mechanism with an NMOS transistor closing the circuit for the valves, however, this new hardware iteration natively integrates error detection mechanisms that were absent in the previous generation. Fault detection is implemented passively at the hardware level using resistor divider networks, as can be seen in Figure 2. These networks continuously monitor voltage potentials at the MOSFET drains, allowing the microcontroller to identify open circuit or disconnected hardware states without needing to actively trigger the valve.

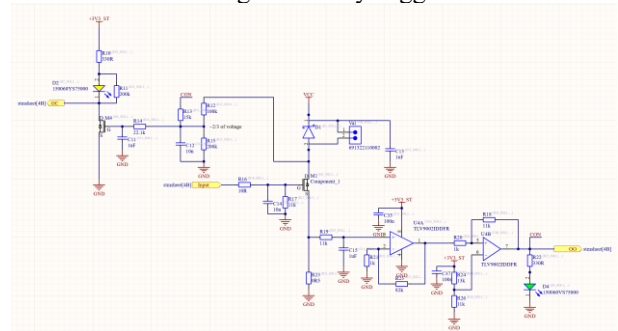


Figure 2: New solenoid valve actuator and failure detection schematic

The proportional ball valves are driven by a custom power stage utilizing an NMOS low side and PMOS high side MOSFET configuration, presented in Figure 3. For the proportional ball valves, functionality is verified at the software level. The STM32G431 periodically commands minute micro actuations and measures the resultant current draw through onboard operational amplifier sensing circuits, similar to those on the solenoid actuators, confirming mechanical responsiveness.

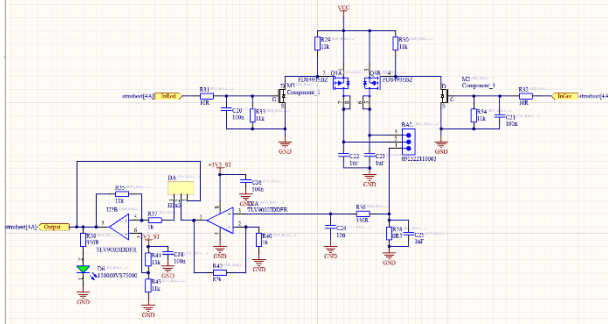


Figure 3: New ball valve actuator and failure detection circuit

The sensor acquisition and communication suites were also modernized to match the processing capabilities of the new architecture. The v6 system relies on an array of four accurate PTE7300 I2C sensors to gather vital engine telemetry, with all data being pulled directly into memory via DMA to avoid CPU bottlenecks, while the old v5 version depended on cheaper alternatives that used the polling method via the same protocol. To support future integration with external Supervisory Control and Data Acquisition (SCADA) environments, the v6 hardware architecture integrates dedicated Controller Area Network (CAN) bus transceivers. However, pending the finalization of the CAN software stack, the current firmware iteration utilizes an APC220 UART transceiver for telemetry and supervisory communication. This maintains protocol continuity with the legacy v5 system while the hardware transitions.

2.2 Testing Methods

The primary objective of the testing phase was to quantify the performance disparity between the legacy synchronous polling architecture and the proposed asynchronous DMA driven approach. Specifically, the experiments were designed to measure maximum loop execution time, system jitter, communication reliability and cpu wait time, or the average time spent waiting during polling, under simulated operational loads.

To ensure a valid comparison, the legacy FADEC v5 required physical modifications to match the diagnostic capabilities of the newer v6 architecture. The v5 architecture was modified to sustain higher loads for ball valve actuation. Because the legacy system natively lacked hardware level connection detection and active actuation verification, equivalent diagnostic circuits were constructed on a breadboard and interfaced with the older hardware. This retrofit included identical resistor divider networks for the solenoid valves and operational amplifier current sensing circuits for the proportional ball

valves. Implementing these physical upgrades guaranteed that both the legacy dual microcontroller setup and the modernized single microcontroller system drove identical electrical loads and processed the exact same analog diagnostic signals during the evaluation.

With hardware parity established, the firmware for both systems was unified into a structurally identical operational sequence. The main control loop was standardized to follow a strict, sequential execution path, which is presented in Figure 4. The cycle initiates by retrieving external supervisory commands, which is immediately followed by the evaluation and actuation of the emergency solenoid valves. Subsequently, the system executes proportional position commands for the ball valves before acquiring engine telemetry from the sensor array. The loop then verifies the actuator diagnostic states and concludes by transmitting the compiled telemetry payload back to the supervisory interface. By forcing both architectures to navigate this exact logical sequence, any measured deviation in execution speed or determinism could be directly attributed to the underlying differences between synchronous peripheral polling and asynchronous memory access.

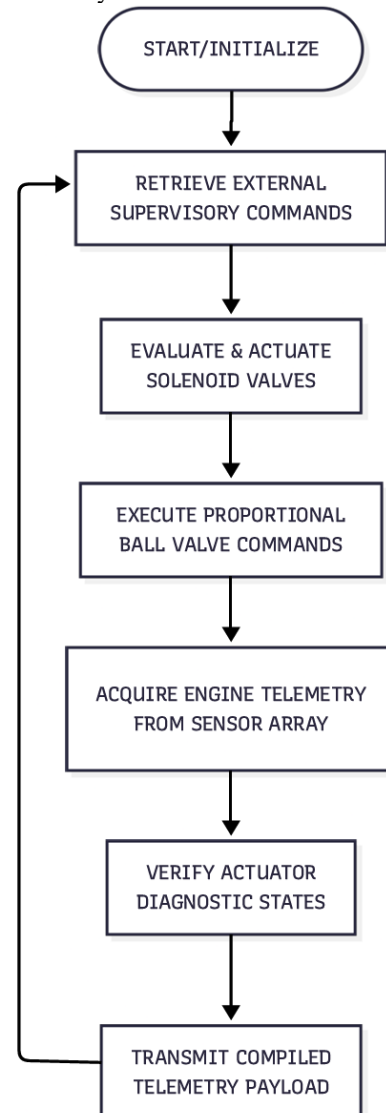


Figure 4: Main loop and flow chart

To conduct the stress test, a Python test bench was configured to deterministically inject Noordung Service Link Protocol (NSLP) communication packets via the UART interface into both microcontrollers at 200 ms intervals.

To capture the performance metrics, dedicated timing functions were embedded directly into the main execution loops of both systems. These onboard routines continuously calculated the execution time of each loop iteration, allowing the system to derive the resulting jitter caused by peripheral blocking and processor stalling. The microcontrollers actively tracked their communication integrity by counting the number of dropped, missed, or incomplete NSLP packets over the duration of the test.

3 Results

Performance logs extracted from the testing sequence demonstrated a substantial disparity in execution speeds. The legacy FADEC v5 system, utilizing a dual microcontroller setup and synchronous peripheral polling, recorded an average loop execution time of 189867 μ s per cycle. Under identical operational loads, the single microcontroller FADEC v6 architecture logged an average loop execution time of 2239 μ s. This represents an execution time reduction of 187628 μ s per loop iteration for the modernized single microcontroller DMA architecture.

System jitter was simultaneously recorded by the internal hardware timers. The legacy v5 architecture demonstrated a maximum measured jitter of 5534 μ s across the testing window. In comparison, the v6 system recorded a maximum system jitter of 4437 μ s. This equates to a jitter reduction of 1097 μ s for the v6 system, establishing a narrower variance band during the main loop.

Communication integrity was tracked during the Python based NSLP injection code, where packets were transmitted to the microcontrollers' receive buffers. Over the standardized testing window, the external test bench injected 92 discrete communication packets into both systems. The legacy v5 internal logs recorded 14 dropped packets, resulting in a packet loss rate of 15.22%. During the identical testing window for the proposed v6 architecture, the microcontroller successfully processed all 92 payloads, resulting in a 0% packet loss rate.

The internal monitoring routines logged the central processing unit active wait times required to sustain the main control loop. Legacy v5 architecture recorded an average CPU waiting time of 11% while managing synchronous peripheral polling and communication between the MCUs. The DMA driven v6 system logged an average active wait time of 0% throughout the entire testing window. This reflects a reduction of 11% in the processor's computational load while successfully processing identical external commands, actuator states, and telemetry arrays.

Version	Loop time [μ s]	Jitter [μ s]	Packets received	Packets lost	Wait Time [%]
V5	189867	5534	78	14	11
V6	2239	4437	92	0	0

Table 1: Results of testing procedure

4 Conclusions

In this paper, an implementation of a modernized, single microcontroller FADEC for throttleable aerospace applications is presented. Notable system upgrades include proportional ball valve actuation, diagnostic control circuits, CAN bus communication, and DMA peripheral processing.

The comparative analysis of the legacy FADEC v5 and the proposed FADEC v6 architectures demonstrates that transitioning from synchronous peripheral polling to asynchronous Direct Memory Access yields improvements in processing speed and communication integrity. However, it also introduces complex compromises regarding relative system determinism. The proposed v6 architecture exhibits a significant reduction in average loop execution time. It decreases the cycle duration from nearly 190 ms to approximately 2.2 ms. In practical aerospace applications, this accelerated execution allows the system to parse incoming telemetry packets and trigger critical actuator responses, including emergency valve shutdowns upon fault detection, magnitudes faster than the legacy architecture. Furthermore, the complete elimination of packet loss in the v6 system directly resolves the 15.22% communication failure rate observed in the v5 architecture under high stress conditions.

The 15.22% communication failure rate observed in the legacy v5 architecture can be directly attributed to UART receive buffer overruns caused by processing latency. The test bench deterministically injected communication packets at 200 ms intervals. Because the synchronous v5 architecture required an average loop execution time of approximately 190 ms, combined with a maximum system jitter of 5.5 ms, the worst-case cycle time routinely exceeded 195 ms. This left a processing margin of less than 5 ms, meaning the CPU was frequently unable to poll and clear the receive buffer before the next packet arrived, resulting in dropped payloads. In contrast, the v6 architecture resolves this fundamentally by utilizing DMA for communication. This allows incoming payloads to be transferred directly into memory in the background, completely decoupling communication reliability from main CPU execution cycles and ensuring a 0% packet loss rate regardless of main loop variations.

This reduction in loop execution time directly impacts the physical response capabilities of the control actuators. Operating at a 2.2 ms average cycle rate provides the time resolution required to process proportional

ball valve commands with lower control latency, a necessary condition for maintaining continuous target fuel-to-oxidizer mixture ratios during dynamic throttling. Furthermore, a 0% packet loss rate ensures that discrete hardware state changes, such as triggering the emergency solenoid valves during a fault condition, are executed within a predictable timeframe. By mitigating the 190 ms delays inherent to the legacy polling architecture, the modernized framework provides the deterministic actuator response required for active fluid management.

This performance gain is compounded by a measured reduction in active computational overhead. In the v5 architecture, the microcontroller expends 11% of its computational bandwidth executing blocking operations to check peripheral registers. By offloading data movement entirely to the hardware level memory controllers, the v6 architecture reduces active CPU waiting time to 0% during the identical control sequence. This transition eliminates processor stalling and reclaims significant computational headroom. It allows the single microcontroller system to process complex, real time throttling algorithms without degrading the primary execution loop.

Despite these advantages, data highlights a variance regarding execution determinism. While the v6 architecture recorded a lower system jitter (4437 μ s) compared to the v5 architecture (5534 μ s), the relative impact of this variance is larger. This measured jitter is attributed to two concurrent hardware factors, the buffering sequence of the APC220 radio unit utilized for supervisory communication, and memory bus contention from the sensor array operating at 400 kHz. During telemetry transmission, the buffer management inherent to the radio module introduces periodic delays. Simultaneously, retrieving data from the four PTE7300 sensors at a 400 kHz clock speed via Direct Memory Access generates continuous memory bus traffic that can briefly stall the processor. Because these hardware behaviors are tied to telemetry transmission windows and high frequency memory access rather than continuous peripheral polling, they cause isolated execution spikes that deviate from the baseline loop time.

This loss of strict determinism naturally extends to sensor data acquisition. In a synchronous polling architecture, the precise timestamp of a sensor reading is inherently tied to the moment of CPU execution. Conversely, in the asynchronous DMA driven v6 architecture, sensor data is continuously updated in background memory arrays. While the system actively timestamps the data upon evaluation within the main loop, the exact microsecond of the physical measurement is decoupled from this software timestamp. This introduces a slight variance in data freshness, as the recorded time reflects the moment of loop processing rather than the instant of hardware acquisition.

However, this time ambiguity must be contextualized within the overall system velocity. Even when combining the average loop execution time with the maximum recorded jitter, the worst-case response cycle for

the v6 system remains under 7 ms. The maximum possible latency of any given sensor reading in the modernized architecture is still nearly 28 times faster than the baseline 190 ms cycle of the legacy v5 system. This reduction in response time dictates that the time variance introduced by DMA is an acceptable tradeoff for the superior fault reaction capabilities of the single microcontroller framework.

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Device for Testing and Development of an Electric Vehicle Charging Station

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Abstract: This paper presents the design and implementation of the Sym-A device. The process of constructing electronics, designing the enclosure, and writing the program code is described in detail [1], [2]. The device is a part of a test system used within the development of Etrek's Inch Core electric charging station software. Additionally, the device is used to test software functionalities and test cases that cannot be reproduced in real world scenarios with the fully assembled station. The logical part of the charger is attached to the test system. The power and measurement part is simulated or emulated by a developed device. Using the platform, the charging process can be tested, and various operational modes of the station can be simulated. All types of charging cables can be configured by manipulating the Proximity Pilot signal. To change the car's charging state, the system manages the Control Pilot signal line intended for communication between the charger and the electric vehicle. The device has an additional practical advantage, allowing arbitrary changes to the charger's behavior, since most peripheral functions are simulated [3]. Thus, real and hypothetical scenarios of the charging station's operation can be tested.

Keywords: electric vehicle charging station; test platform; peripheral emulation; Control Pilot; embedded system

1 Introduction

Developing embedded software for electric vehicle charging stations requires testing control algorithms, communication interfaces, and peripheral responses. Using a fully assembled system is less practical because all equipment is required and the user may be exposed to hazardous mains voltage. Some abnormal conditions are also difficult to recreate with physical sensors and actuators.

A dedicated test platform simplifies development by connecting the actual high-level control logic to an environment in which the remaining peripheral functions are simulated or emulated [3]. The emulated system provides the signals and communication responses required for software operation without switching high-power loads. Related work includes

hardware-in-the-loop platforms for charging-station control and firmware [4] and mobile devices for testing AC/DC charging infrastructure communication [5].

This paper presents the Sym-A test platform, designed for the development and functional testing of electric vehicle charging station software. The platform connects to the control unit under test and emulates the peripheral signals and communication interfaces required for its operation. It also simulates the connection of an electric vehicle and a charging cable by controlling the Control Pilot (CP) and Proximity Pilot (PP) signal lines.

2 Test Platform Concept

2.1 General Operating Principle

The unit under test contains the high-level logic responsible for managing the charging process and communication with the remaining parts of the system. During development, it is connected directly to Sym-A instead of being installed in the complete charging station.

Sym-A supplies the connected unit and provides the electrical and communication interfaces that it expects. The platform emulates digital inputs and outputs, serial communication devices, measurement-related communication, and selected sensor and actuator responses. The control software can therefore initialize and operate as if it were connected to the complete system.

The purpose of the platform is not to reproduce the physical transfer of electrical energy. Instead, it reproduces the information exchanged between the high-level logic and the peripheral hardware, including signal levels, register values, communication messages, interrupt signals, and feedback states.

2.2 Functional Requirements

The main requirements were simulation of the vehicle state through the CP signal, simulation of cable presence and current capability through the PP signal, emulation of digital peripheral devices connected through I²C, generation of digital input states and interrupt signals, and observation of control outputs followed by the corresponding simulated feedback.

The platform also supports serial and measurement-related communication, programming, debugging, reset, and power cycling.

Software-configurable peripheral behavior allows the same hardware to represent normal, boundary, and fault conditions, including delayed, invalid, missing, or corrupted responses.

3 Hardware Design

3.1 Overall Hardware Architecture

Sym-A is implemented on one printed circuit board and consists of several functional blocks. The central component is a Texas Instruments CC1314 microcontroller, which controls the simulation hardware and executes the peripheral emulation software.

Communication with a host computer is provided through a USB-C connector. A three-port USB 2.0 hub distributes the connection between the integrated debugging interface, a multi-channel USB-to-UART converter, and an additional USB connection intended for the attached control unit.

The FT4232HL provides four UART channels. One channel is used for the Sym-A command-line interface, two channels are used for communication with and programming of the connected control unit, and the fourth channel is routed to an external connector. LEDs indicate transmit and receive activity.

An integrated XDS110 interface programs and debugs supported Texas Instruments microcontrollers and can connect to Sym-A or the attached control unit. RS-485 supports external devices or their software simulation, while I²C, SPI, and additional digital connections support emulated peripherals. Figure 1 shows the overall hardware architecture.

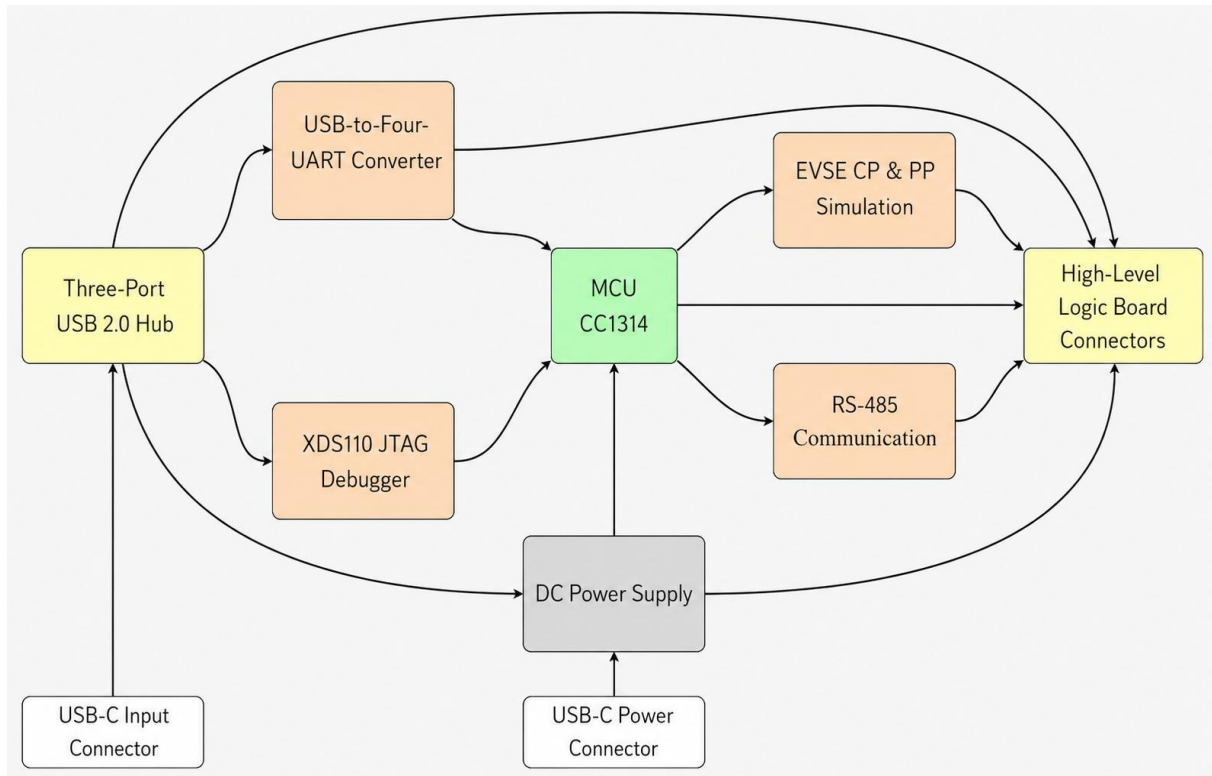


Figure 1: Block diagram of the Sym-A hardware architecture.

3.2 Control Pilot and Proximity Pilot Simulation

Sym-A simulates the electric vehicle side of the CP interface by connecting different resistance values between the signal line and the reference potential. The basic circuit includes the diode used on the vehicle side and several selectable resistance paths. Most resistance values are generated by a digital potentiometer with two adjustable channels, a maximum resistance of 20 k Ω , and 256 programmable steps.

Solid-state relays connect or disconnect individual parts of the simulation circuit. The microcontroller can therefore select standard charging states and create additional test conditions. The implemented functions include an open CP line, a short circuit to the reference potential, a simulated short-circuited vehicle diode, and voltage levels immediately above or below the limits used by the control logic.

Capacitive and inductive elements can also be inserted into the CP signal path. These components intentionally distort the waveform

and introduce smaller oscillations or disturbances. This makes it possible to observe the operation of the communication and control software when the signal conditions are not ideal.

The PP line is simulated by a similar resistance-selection principle. The connected resistance represents the connection type and current capability of the charging cable. Configurations for 13 A, 20 A, and 32 A cables are implemented for both a socket and an attached-cable arrangement. The platform can also generate an open line, a low-resistance short-circuit condition, and resistance values immediately above or below the expected ranges.

For verification, the digital potentiometers can be disconnected from the external signal lines and connected to an internal measurement circuit. The resistance is estimated from the voltage of a resistor divider measured by the microcontroller analog-to-digital converter.

3.3 Power Supply and Physical Implementation

The platform is powered through USB-C. One connector combines power and USB data, while a second connector is intended only for auxiliary power. The board normally uses the data connection as its supply. When additional power is connected, an internal circuit changes the active source.

The 5 V input is converted to 3.3 V for the digital electronics and the attached control unit. A boost converter generates 15 V for the CP simulation circuit and the digital potentiometers. During hardware verification, the measured ripple of both generated voltages was approximately 10 mV.

The printed circuit board has four copper layers. The outer copper thickness is 35 μm , and the two inner layers use 17.5 μm copper. One internal layer is a continuous ground plane, while unused areas on the other layers are also filled with grounded copper. USB differential pairs were designed for a differential impedance of 90 Ω , and the radio-frequency transmission line was designed for 50 Ω .

The completed board measures 140 mm $\times$ 83 mm and is mainly assembled with surface-mount components. The enclosure follows the rectangular board shape and was produced by selective laser sintering. It supports the printed circuit board, mounting spacers, and spring-contact inserts while leaving connectors and measurement points accessible. Ten printed circuit boards and ten matching enclosures were prepared for the initial series.

4 Embedded Software

4.1 Software Architecture

The embedded software was written in C for the CC1314 microcontroller. The implementation uses SimpleLink Low Power Software Development Kit version 7.41.0.17 [2] and the TI-RTOS real-time operating system [1].

The software is divided into independent functional modules. Each module manages a specific part of the platform and can contain one or more real-time operating system tasks. A central module manager initializes the other modules and provides information

about their state, allocated memory, task execution, supply voltage, and microcontroller temperature.

The main modules provide serial communication, I²C device emulation, electric vehicle simulation, SPI emulation, and Sub-1 GHz communication. Serial communication, I²C emulation, and vehicle simulation form the main implemented functions; the remaining modules support current needs and further software expansion. Figure 2 shows the modular architecture.

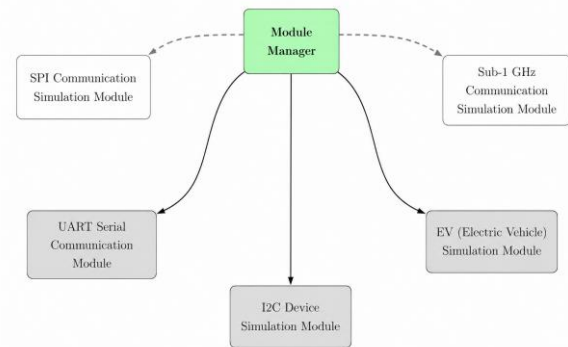


Figure 2: Block diagram of the Sym-A software architecture.

4.2 I²C Peripheral Emulation

The Sym-A microcontroller uses two I²C buses. One controls devices located on the test platform, while the other is used to emulate peripheral devices expected by the attached control unit. On the emulation bus, the microcontroller operates as a subordinate device rather than as the communication controller.

The available high-level software support did not provide all functions required for this operating mode. A dedicated low-level driver was therefore implemented by using the general peripheral libraries available for the microcontroller.

The driver uses an interrupt routine that is triggered when the external controller accesses the configured I²C address. The routine determines whether the controller is writing a register address, writing register data, or requesting data from a register. It then calls the corresponding read or write function of the simulated device.

The emulated input-output expander maintains configuration, input, output, status, and interrupt registers. When the control unit modifies an output register, the software detects the change and executes the corresponding simulated response. When an emulated input changes, the platform updates the appropriate register and can generate an interrupt signal toward the control unit.

The low-level communication driver is separated from the higher-level model that defines the behavior of individual inputs and outputs. Different test scenarios can therefore use the same register and communication implementation while producing different peripheral responses.

4.3 Electric Vehicle Simulation and Command-Line Interface

The electric vehicle simulation module controls the circuits connected to the CP and PP lines. It communicates with the digital potentiometers and the input-output expander through the internal I²C bus. The module selects the required resistance values and controls the solid-state relays used to configure the signal paths.

The user can start or stop a simulated charging sequence, select a cable configuration, change the simulated vehicle state, and activate individual fault conditions. The module can also coordinate its actions with other peripheral emulation modules. A scenario can therefore combine a change on a pilot signal with a selected digital input or communication response.

Sym-A is controlled through a command-line interface available over UART at 115200 baud, with eight data bits and one stop bit. Commands are provided for charging simulation, cable selection, CP states, signal faults, digital potentiometer values, and manual access to the registers of the emulated I²C device.

Additional commands report task states, memory use, heap status, supply voltage, and microcontroller temperature. The user can also reset the Sym-A platform and power-cycle the connected control unit. A command-

line interface was selected because the platform is intended for technical users and because it gives direct access to low-level test parameters.

5 Experimental Results and Discussion

The completed boards were verified incrementally during hardware bring-up. The 3.3 V and 15 V power supplies operated correctly, with voltage ripple of approximately 10 mV.

The USB hub and the four-channel USB-to-UART converter were tested after connection to a personal computer. The UART channels were verified by loopback connections. Characters entered in a serial terminal were received correctly, and the corresponding transmit and receive indicators operated as expected.

The integrated debugging interface was first tested through its separate USB connection and was then connected to the internal USB hub. It successfully provided access to the microcontroller through JTAG. The CC1314 was programmed with a basic test application, after which serial communication, I²C communication, light-emitting diode control, and the solid-state relay outputs were verified.

The completed platform combines the functions required for connecting, supplying, communicating with, programming, and debugging the high-level control logic. The same device provides software-controlled peripheral responses and simulation of the electric vehicle signal interface.

A practical advantage of the developed approach is that software can be developed without a complete charging station and without exposing the user to mains voltage. Peripheral behavior and selected fault scenarios can be changed through software instead of physically modifying sensors, actuators, or communication devices.

The platform does not reproduce the actual transfer of electrical energy. In addition, the planned SPI measurement emulation and Sub-1 GHz communication functions can be

expanded further in software. The mechanical attachment of the tested board requires simultaneous alignment with the connectors and spring contacts. A larger fixture using only spring contacts could simplify mounting, but it would increase the size and cost of the system.

6 Conclusions

A compact embedded platform for the development and testing of electric vehicle charging station control software was designed and implemented. Sym-A connects to the actual high-level control logic and replaces the peripheral hardware required for its operation with programmable simulation circuits and communication interfaces.

The system integrates USB communication, multiple UART channels, RS-485, I²C peripheral emulation, an XDS110 debugging interface, power supplies, and circuits for CP and PP simulation. Its embedded software is based on TI-RTOS and uses a modular architecture that separates communication, peripheral emulation, and electric vehicle simulation functions.

The implemented functions support normal operating states, boundary values, and selected fault scenarios. The completed hardware was brought into operation, and the power-supply, communication, debugging, and simulation-related functions were verified. Further development can extend the software support for measurement-related and Sub-1 GHz communication and can improve the mechanical mounting of the control unit under test.

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Reliability Challenges of Commercial Power p-Channel VDMOS Under NBT Stress

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Power p-channel VDMOS transistors are widely used in switching, power management, automotive, and industrial applications, where long-term reliability and stable operation are of critical importance. Among the degradation mechanisms affecting these devices, negative bias temperature instability (NBTI) is recognized as one of the most significant reliability concerns, leading to gradual variations in electrical parameters during operation. Such changes can alter device performance and eventually influence the behavior of circuits in which these transistors are employed. This paper investigates the impact of NBT induced degradation on commercial power p-channel VDMOS transistors from the perspective of practical applications. The study combines accelerated negative bias temperature stressing with comprehensive thermal and circuit level characterization. Infrared thermography was used to monitor temperature evolution and self-heating behavior under various load driving conditions, enabling evaluation of the influence of prior electrical degradation on thermal response. In parallel, the impact of NBTI on circuit operation was analyzed through the characterization of a CMOS inverter incorporating previously stressed transistors. Special attention was devoted to correlating threshold voltage shifts with changes in self-heating, transfer characteristics, and dynamic performance parameters.

The experimental results show that NBT induced threshold voltage shifts lead to increased self-heating during high current operation due to changes in channel resistance and power dissipation. Furthermore, degradation affects the transfer and switching characteristics of CMOS inverter circuits, resulting in measurable variations in circuit performance. The presented findings provide a deeper understanding of the practical consequences of NBTI degradation and highlight the necessity of considering related reliability effects during the design, optimization, and lifetime assessment of power VDMOS based electronic systems.

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ABSTRACT



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Impact of Prior NBT Stress on the Self-Heating Behavior of Power P- and N-Channel VDMOS Transistors

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Abstract: Self-heating represents one of the major reliability concerns in power VDMOS transistors operating under elevated current conditions. Since these devices are frequently exposed to electrical and thermal stresses during their lifetime, understanding the influence of prior degradation on their thermal behavior is essential for accurate reliability assessment. In this paper, the self-heating characteristics of commercial p-channel and n-channel power VDMOS transistors were investigated with special emphasis on the effects of previous negative bias temperature (NBT) stressing. The analyzed devices were subjected to either static or pulsed NBT stress, followed by stabilization procedures involving spontaneous recovery and thermal annealing. Subsequently, infrared thermography was used to monitor temperature evolution during operation under different drain current levels and gate drive conditions. The thermal response of stressed devices was compared with fresh transistors. The obtained results revealed a clear dependence of self-heating on the prior stress history of the devices. For both transistor types, NBT stressed samples exhibited higher temperature rise than fresh devices, while the largest temperature increase was consistently observed in transistors previously exposed to static NBT stress. In addition, n-channel devices reached significantly higher operating temperatures than p-channel counterparts under identical test conditions. These observations are associated with NBT induced threshold voltage shifts and corresponding changes in channel resistance and power dissipation mechanisms.

Keywords: Power VDMOSFETs; Negative Bias Temperature Instability (NBTI); Self-Heating Effects (SHE); Threshold-Voltage Shift; Infrared Thermography

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1 Introduction

Power Vertical Double-Diffused MOSFETs (VDMOSFETs) are widely utilized in automotive and industrial electronic systems due to their high current capability, low on-state resistance, and favorable switching performance. Typical applications include power converters, motor drives, switching power supplies, and various control and protection

circuits [1, 2]. Despite their inherent robustness, long-term operation under electrical and thermal stress may significantly affect their electrical characteristics and, consequently, device reliability. Among the degradation mechanisms relevant to power VDMOS transistors, bias temperature instability (BTI) and self-heating effects (SHE) are of particular importance [2, 3].

Self-heating originates from power dissipation within the device and becomes increasingly pronounced at high drain currents and during switching operation. The resulting increase in junction temperature can modify the electrical characteristics of the transistor and accelerate degradation mechanisms. Although appropriate thermal management can reduce these effects, the use of heatsinks may be constrained in compact electronic systems, particularly in automotive applications [3, 4]. Therefore, understanding the thermal response of power devices under realistic operating conditions is essential for reliable circuit design, as initially investigated in [3].

Negative bias temperature instability (NBTI) represents another important reliability concern. Under negative gate bias and elevated temperature, charge trapping in the gate oxide and the generation of interface traps lead to a threshold voltage shift and the corresponding degradation of device characteristics [2, 3]. Although NBTI is predominantly associated with p-channel devices, NBT stress induced degradation can also be relevant to n-channel power VDMOS transistors. In high-speed switching applications, a negative gate voltage may be applied to accelerate transistor turn-off, exposing n-channel devices to conditions that can induce similar degradation effects [5]. The relatively thick gate oxide of power VDMOS structures allows operation at high gate voltages, but also makes these devices susceptible to oxide-related reliability phenomena. In practical power-electronic applications, electrical and thermal degradation mechanisms do not occur independently. Gate signals with different rise and fall times (t_{rise} and t_{fall}) determine the switching dynamics and power dissipation and may consequently influence both NBTI degradation and device self-heating [6]. Therefore, evaluating the thermal behavior of previously stressed devices under realistic switching conditions can provide valuable insight into the relationship between accumulated electrical degradation and subsequent device operation.

In this paper, the self-heating behavior of p- and n-channel power VDMOS transistors with different prior loading stress is experimentally

investigated. Fresh devices are compared with samples previously subjected to static and pulsed NBT stress, followed by recovery and thermal annealing. The influence of drain current, gate signal rise and fall times, and prior NBT stress on the temperature increase is evaluated using infrared thermography.

2 Experimental Setup and Measurement Procedure for Static and Pulsed NBT Stress

The experimental investigations presented in this paper were primarily conducted on power VDMOS transistors, including both p-channel and n-channel devices. The studied components are commercially available as IRF9520 and IRF510, originally manufactured by International Rectifier and currently offered by Vishay Siliconix. These devices are fabricated using standard poly-Si technology and have a relatively thick gate oxide of approximately 100 nm, which is characteristic of power MOSFETs and significantly thicker than oxides in advanced CMOS technologies.

All devices are encapsulated in a TO-220 package with three terminals (drain, gate, and source, with the source shorted to the bulk). Their robust structure and high breakdown voltages make them suitable for accelerated stress testing under elevated electric fields. Due to the thick gate oxide, accelerated NBT stress experiments require the application of gate voltages significantly higher than those used in standard operation, typically in the range of -30 V to -50 V, corresponding to electric fields on the order of several MV/cm. Both static and pulsed NBT stress experiments were conducted in a controlled laboratory environment. The core of the experimental setup consists of a high-voltage DC power supply, a temperature chamber, supporting electronic circuitry, and measurement instrumentation. For static NBT stress, a programmable DC power supply (Agilent 6645A) was used to apply a constant gate voltage in the required range. Multiple devices (typically 6-8) were stressed simultaneously, mounted on a custom designed board. During stress, the drain and source terminals were shorted and

grounded, while the gate terminal was under negative bias. Figure 1 represents the photo of the stress setup.

The temperature conditions were maintained using a temperature chamber, typically set to 175 °C, which is the temperature frequently used to accelerate degradation processes. Due to the long duration of stress experiments (commonly up to 168 hours), careful monitoring of electrical and thermal stability was required, as well as precautions against potential issues such as contact degradation or power interruptions. In contrast, pulsed NBT stress introduces time dependent gate bias conditions, requiring additional instrumentation. A signal generator (Agilent 33521A) was used to generate rectangular pulse signals with controlled amplitude, frequency, and duty cycle. These signals were used to drive a switching transistor, which acts as a gate control element, enabling periodic application of high voltage stress to the tested devices. The switching operation ensures that the gate voltage alternates between a stress phase (high electric field) and a recovery phase (zero bias).



Figure 1: The experimental stress setup.

The pulsed stress setup also includes an oscilloscope for real time monitoring of the applied signals, ensuring accurate waveform delivery to the device under test. A high power resistor is incorporated to limit current, and appropriate heat sinking is used for the switching transistor due to increased power dissipation under high frequency operation. The stress conditions typically involve frequencies in the kHz range, with duty cycles adjusted to study the influence of dynamic stress on device degradation.

Despite differences in stress application, the measurement procedure remains consistent

for both static and pulsed experiments. At predefined intervals, the stress is interrupted, and the devices are removed from the temperature chamber and cooled to room temperature (~25 °C). Cooling is assisted by forced air (fan) and heat sinks, while temperature stabilization is verified using an infrared thermometer. Electrical characterization was performed using a Source Measure Unit, specifically the Keysight B2901A, controlled via a computer interface, as can be seen in Figure 2. Transfer I - V characteristics are measured over a wide gate voltage range to capture both subthreshold and above-threshold regions. During measurement, the drain and gate terminals are shorted to ensure operation in the saturation regime, while the source is grounded. To minimize external noise, measurements are conducted within an enclosure acting as a Faraday cage.



Figure 2: The experimental measurement setup.

The acquired data are further processed using custom scripts implemented in Octave, enabling automated extraction of key electrical parameters. The Subthreshold Midgap (SMG) technique is applied to determine threshold voltage shifts, which are essential for understanding the degradation mechanisms induced by NBT stress.

3 Experimental setup for self-heating measurements

The self-heating behavior of power VDMOS transistors was investigated using a laboratory setup designed to emulate realistic operating conditions. The experiments were conducted on both fresh and previously stressed devices, with the transistor configured as a switch in a circuit with an active load, representing typical applications such as motor

control. The experimental setup consists of several key components, shown in Figure 3. Gate control signals were generated using a programmable function generator (Agilent 33521A), enabling precise adjustment of amplitude, frequency, and waveform shape. The drain current was regulated using an electronic load (Rigol DL3021), while a DC power supply (GW Instek PSP-2010) provided a stable supply voltage. Signal integrity and waveform characteristics were verified using a digital oscilloscope (Rigol DS1104Z).

Self-heating measurements were performed at constant drain currents of 0.5 A, 1 A, 1.5 A, and 2 A, selected to ensure observable thermal effects without approaching the maximum rated current of the devices. Each measurement cycle consisted of a heating phase (~6 minutes), during which the device was in active state, followed by a cooling phase (~6 minutes), with no applied signal. This approach enabled clear observation of both thermal buildup and cooling processes.

Temperature monitoring was carried out using a thermal imaging camera (FLIR E8), controlled via software (FLIR Thermal Studio). The camera provides high sensitivity and accuracy, allowing reliable detection of temperature variations during operation. To ensure measurement accuracy, ambient conditions such as temperature and humidity were monitored using a digital meter (CEM DT-321S). Experiments were conducted under controlled laboratory conditions, with ambient temperature maintained at approximately $24 \pm 1^\circ\text{C}$ and relative humidity at $35 \pm 4\%$. The applied gate signals had amplitudes of -10 V for p-channel and +10 V for n-channel transistors, with a frequency of 1 Hz and a duty cycle of 50%. To investigate the impact of switching dynamics on self-heating, three different rise and fall times were used (5 ns, 100 ns, and 250 ns).

Temperature data were extracted from thermal images by analyzing the maximum temperature within a defined region of interest corresponding to the entire TO-220 package surface. This approach is justified by the efficient thermal coupling between the chip and

the package. All measurements were performed under carefully controlled and repeatable conditions to ensure reliability and comparability of results.



Figure 3: The IR measurement setup.

4 Investigation of Sample Temperature Variations as a Function of Prior Stress Conditions

The components, subjected to different types of electrical and/or thermal stress in this study, are transistors commonly encountered in practical applications, either as active components of electronic systems or as back-up components intended for use in the event of primary component failure. It is well established that such stress conditions can induce degradation of electrical characteristics and device parameters, thereby directly affecting component reliability and operational lifetime. However, for a comprehensive assessment of their applicability under normal operating conditions, it is necessary to investigate how stress induced changes affect device behavior during regular operation. The analysis included a comparison between fresh devices and devices previously subjected to NBT stress under both static and pulsed stress conditions. It is important to emphasize that thermal annealing following the NBT stress phase represents a necessary step for ensuring the validity and reliability of the subsequent self-heating experiments. If the self-heating measurements had been initiated immediately after NBT stress, the device threshold voltage would have continued to change due to the

temperature increase induced by self-heating. Consequently, it would have been difficult to distinguish between changes originating from post stress recovery and those directly associated with the self-heating process. By incorporating spontaneous recovery and thermal annealing stages into the experimental procedure, a certain degree of device parameter stabilization was achieved. In this manner, the effects associated with self-heating were effectively separated from those arising from thermal annealing.

Two different operating frequencies were applied in the experimental procedure for practical reasons. During pulsed NBT stress, a frequency of 10 kHz was selected to reproduce operating conditions representative of power VDMOS transistor applications. Following NBT stress, the frequency was reduced to 1 Hz during the self-heating experiments to allow sufficient time for thermal stabilization and to clearly resolve the cooling process within each operating cycle. This lower frequency modulation enabled the infrared camera to accurately capture the temperature rise and subsequent spontaneous thermal recovery of the device. Such a low operating frequency may also be encountered in practical applications, for example, in automotive windshield-wiper control systems [7].

Measurements were performed on multiple samples, and the graphs (Figure 4 and Figure 5) present the mean values obtained from these measurements. The results provide a detailed representation of the device temperature variations obtained for a gate control signal with rise and fall times of 5 ns, 100 ms and 250 ns. Results show the temperature variation of power VDMOS transistors for different gate signals and different stress histories, at an applied drain current of 1.5 A for p-channel devices (Figure 4), while the corresponding results for n-channel transistors at an applied drain current of 2 A are presented in Figure 5. It can be observed that the lowest temperature rise occurs in the un-stressed devices, whereas the highest temperature increase is recorded for the samples previously subjected to static NBT stress.

The highest temperature rise was observed in devices driven by gate signals with rise and fall times of 250 ms, whereas the lowest thermal response was recorded for signals with t_{rise} and t_{fall} values of 5 ns. This behavior can be attributed to the slower transition of the transistor from the cut-off region to the saturation region, resulting in increased power dissipation, since a constant current is maintained through the device during the measurement. A comparison of the results presented in Figure 4 and Figure 5 clearly indicates that the temperature differences between the two graphs are also influenced by the different drain current levels applied during the measurements.

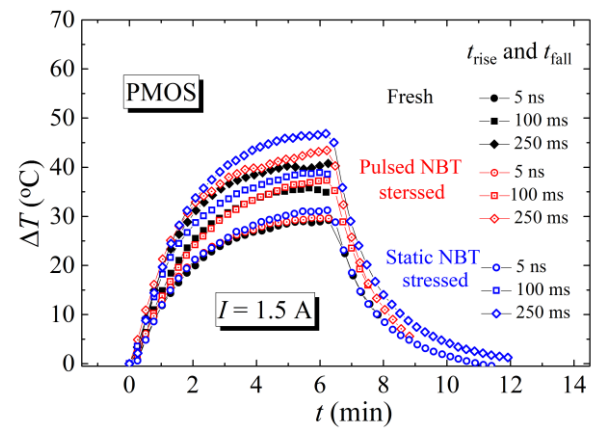


Figure 4: T behavior of p-channel power VDMOSs at a drain current of 1.5 A, considering different gate voltage transition times and device stress histories [3].

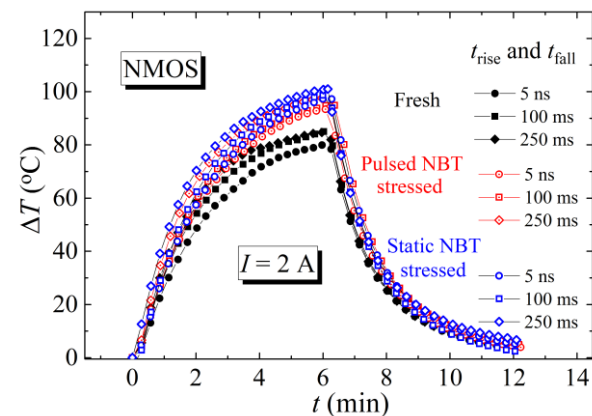


Figure 5: T behavior of n-channel power VDMOSs at a drain current of 2 A, considering different gate voltage transition times and device stress histories.

The analysis confirmed that, although the total signal period remained constant, increasing t_{rise} and t_{fall} effectively modifies the actual duty cycle. For very short t_{rise} and t_{fall} values (5 ns), the gate waveform can be considered rectangular, and the nominal duty cycle of 50% is therefore maintained. However, for longer t_{rise} and t_{fall} values (100 ms and 250 ms), the effective conduction time, defined as the time interval during which the gate voltage exceeds the threshold voltage and the transistor remains in the conducting state, is altered [7, 8].

This effect becomes even more pronounced following NBT stress due to the stress induced threshold voltage shift. In the p-channel transistor, the threshold voltage magnitude increases, (in absolute value), whereas in the n-channel transistor, the threshold voltage decreases. These changes additionally affect the effective conduction interval during which current flows through the transistor and eventually the self-heating [3, 7, 8] (Figure 6).

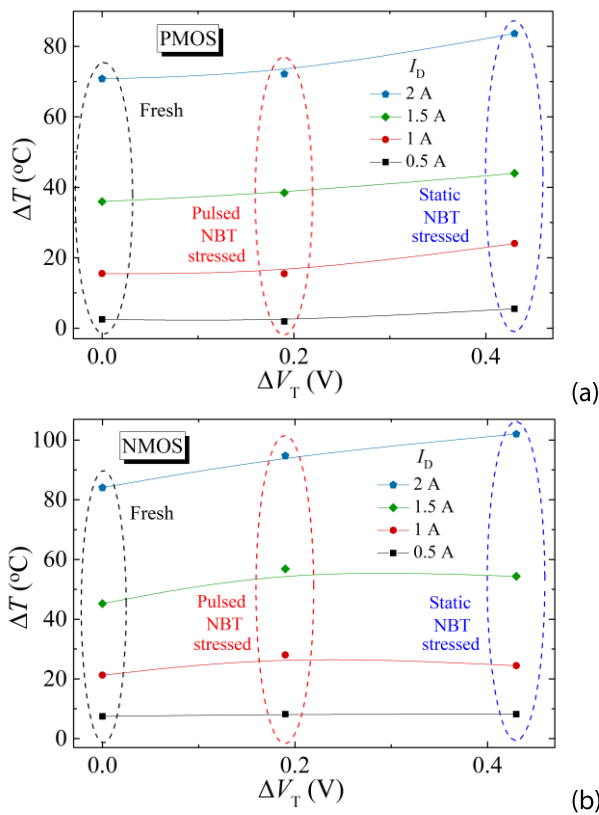


Figure 6: Temperature change as a function of threshold voltage changes for fresh, pulsed NBT stressed, and static NBT stressed power VDMOS transistors operating at drain

currents of 0.5 A, 1 A, 1.5 A, and 2 A: (a) p-channel and (b) n-channel.

Consequently, the conduction time is reduced for the p-channel transistor, whereas it is increased for the n-channel transistor [8-11]. The maximum temperature rise, ΔT , measured after 6 min of self-heating in NBT stressed p-channel and n-channel transistors, at constant drain currents of 0.5 A, 1 A, 1.5 A, and 2 A, with a pulsed gate signal characterized by rise and fall times of 100 ms, are presented in Figure 6, (a) and (b) respectively.

5 Conclusions

This study investigated the self-heating behavior of p- and n-channel power VDMOS transistors with different prior load stress. The results demonstrate that prior NBT stress significantly affects the subsequent thermal response of the devices. Fresh transistors exhibited the lowest temperature rise, whereas the most pronounced self-heating was generally observed in devices previously subjected to static NBT stress. The temperature increase was strongly dependent on the drain current and gate signal dynamics. Also, higher drain currents and longer rise and fall times resulted in more pronounced self-heating due to increased power dissipation and changes in the effective conduction interval. This effect becomes particularly relevant after NBT stress due to the stress induced threshold voltage shift. Overall, the results confirm that the thermal behavior of power VDMOS transistors depends not only on instantaneous operating conditions but also on their previous stresses. Therefore, the combined effects of NBT induced degradation, drain current, and switching dynamics should be considered when evaluating the reliability of power VDMOS devices in practical applications.

6 Acknowledgments

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Impact of Gamma Radiation on Breakdown Voltage Stability and Reliability of Gas-Filled Surge Arresters from Different Manufacturers

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Abstract: Gas-filled surge arresters (GFSAs) are widely used in electronic and power systems to protect against transient overvoltages. Their operation is based on electrical breakdown in a gas medium, which exhibits inherently stochastic behavior. This study investigates the influence of gamma radiation on the breakdown voltage stability and reliability of commercially manufactured GFSAs. Experimental measurements were performed under identical operating conditions, with and without additional gamma irradiation from a radium source. For each applied voltage increase rate, 1000 breakdown voltage measurements were recorded, providing a statistically significant dataset for reliability analysis. The results were evaluated using descriptive statistical methods, focusing on the dependence of mean breakdown voltage on the voltage increase rate. Static breakdown voltage was determined using the dynamic method and linear regression analysis. Gamma irradiation caused a slight reduction in the static breakdown voltage for all tested surge arresters. However, the changes were relatively small, indicating that the devices maintain a high degree of electrical stability under radiation exposure. Experimental distributions were modeled using the Weibull distribution, showing excellent agreement with measured data, confirmed by high correlation coefficients and Pearson's χ^2 goodness-of-fit test. Overall, the investigated GFSAs demonstrate stable electrical characteristics and high reliability under gamma radiation, confirming their suitability for surge protection in radiation-prone environments, including industrial facilities, aerospace platforms, and military systems.

Keywords: Surge arresters; breakdown voltage; gamma radiation; reliability

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1 Introduction

Transient overvoltages are a leading cause of failure in modern electronic and power systems. Caused by lightning strikes, switching events, electrostatic discharge, or electromagnetic interference, these voltage surges can quickly degrade or permanently destroy sensitive equipment. As electronic devices continue to shrink and become more tightly

integrated, robust overvoltage protection has become critical across industrial automation, telecommunications, aerospace, transportation, and defense systems [1].

A range of surge protection devices exists to counter these risks [2]. Transient voltage suppressor (TVS) diodes offer extremely fast re-

sponse times, making them ideal for low-voltage electronic circuits exposed to rapid transients [3], [4]. Metal oxide varistors (MOVs) excel at absorbing high energy and are widely used in power distribution, though their performance degrades over repeated surge events. Gas-filled surge arresters (GFSAs), also known as gas discharge tubes (GDTs) [5], combine high surge current capacity, low capacitance, excellent insulation resistance, and very low on-state resistance. These features make them particularly well-suited for safeguarding signal interfaces, communication lines, and sensitive electronics against severe transient spikes.

A GFSAs operates through electrical breakdown across a gas-filled electrode gap [2], [6], [7]. Unlike solid-state semiconductor devices, the breakdown process in GFSAs is inherently stochastic, depending on initial charge carrier availability, gas ionization dynamics, electrode geometry, gas mix, pressure, and environmental factors. Because of this, the breakdown voltage cannot be captured by a single fixed value and requires statistical analysis [8], [9]. Prior research shows that Weibull statistics offer an effective framework for modeling breakdown voltage distributions and assessing GFSAs reliability under various conditions [10]–[12].

Significant effort has also gone into understanding how ionizing radiation impacts electronic and gas-filled components [3], [4], [13]. Gamma radiation alters gas ionization dynamics, which can shift pre-breakdown currents, delay times, and breakdown voltages [13], [14]. While radiation effects are well documented for semiconductor devices (such as TVS diodes and power transistors) and general gas-discharge components, direct side-by-side evaluations of commercially available GFSAs from different manufacturers under gamma irradiation remain limited, even as demand grows in nuclear facilities, aerospace platforms, particle accelerators, and military applications.

Building on these insights [13]–[17], this paper examines how gamma irradiation affects the breakdown voltage stability and overall reliability of two commercial gas-filled surge arresters. We measured breakdown voltages under identical operating conditions both with and without gamma exposure. Using descriptive metrics and Weibull distribution analysis, we statistically evaluated the results to determine the impact of radiation on device performance and long-term reliability.

2 Components and Method

In this study, we evaluated the reliability of gas discharge surge arresters from two manufacturers (Littelfuse [18] and CITEL [19]) both rated for a nominal operating voltage of 230 V, under exposure to gamma radiation. The radiation was provided by a sealed educational radium-226 source with an activity of approximately 12 kBq.

Educational Ra-226 sources are low-activity, sealed radioactive sources commonly used in laboratory demonstrations and radiation research. They deliver a stable, continuous gamma flux ideal for controlled irradiation experiments, detector calibration, and radiation-effects studies on materials and electronics. Because Ra-226 has a long half-life of roughly 1,600 years, the emission remains virtually constant over long testing periods. Further details on the experimental setup are available in our previous work [13], [16].

Because breakdown voltage in gas-filled surge arrester is inherently stochastic, identical testing conditions yield varying results. To build a statistically robust dataset, we recorded 1,000 breakdown events for each voltage ramp rate. Fig. 1 illustrates the static breakdown voltage distribution for the Littelfuse sample. We applied this same procedure to the CITEL samples; the resulting metrics are summarized in Table 1.

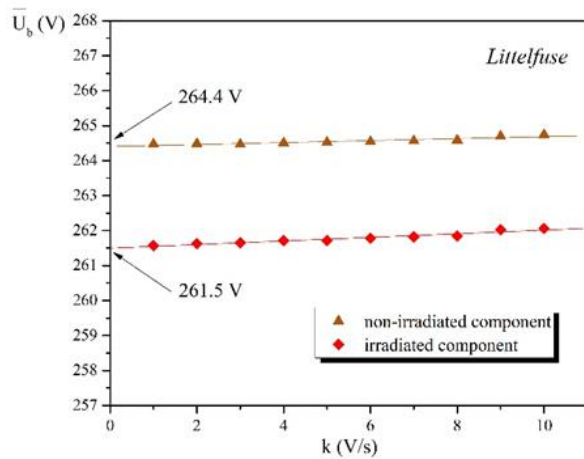


Figure 1: Dependence of the mean breakdown voltage on the voltage increase rate for Littelfuse GFSA.

Table 1: Static breakdown voltage values.

Component	Non-irradiated	Irradiated
Littelfuse	264.4	261.5
CITEL	236.6	234.2

The static breakdown voltage was estimated using the dynamic method by increasing the applied voltage in constant-amplitude steps until breakdown occurred. The voltage increase rate was defined as $k = U_p/t_p$, where U_p is the voltage increment and t_p is the step duration, with investigated rates from 1 V/s to 10 V/s.

The static breakdown voltage was obtained by linear regression of the mean breakdown voltage versus k . Since the dynamic breakdown voltage approaches the static value as $k \rightarrow 0$, the intercept at $k=0$ was taken as the estimated static breakdown voltage. Fig. 2 shows the experimental data and fitted lines, with and without irradiation, demonstrating excellent agreement for all investigated arresters.

The estimated values of the static breakdown voltage are summarized in Table 1. For the CITEL arrester, the static breakdown voltage decreased from 236.6 V to 234.2 V after exposure to gamma radiation. A similar trend was observed for the Littelfuse arrester, where the estimated value decreased from 264.4 V to 261.5 V. These results indicate that gamma ir-

radiation causes a reduction in both the dynamic and static breakdown voltages, although the magnitude of this effect not depends on the arrester type. The reduction of the estimated static breakdown voltage was 2.4 V for the CITEL arrester, and 2.9 V for the Littelfuse arrester. This behavior is similar in both cases and provides the acceptable stability of the breakdown voltage among the tested devices.

A more detailed statistical evaluation of the measurements is presented in Fig. 2, where the mean value, median, minimum, maximum, standard deviation, and the 99th percentile are shown for each voltage increase rate. As a representative example, the gas discharge tube manufactured by Littelfuse was selected.

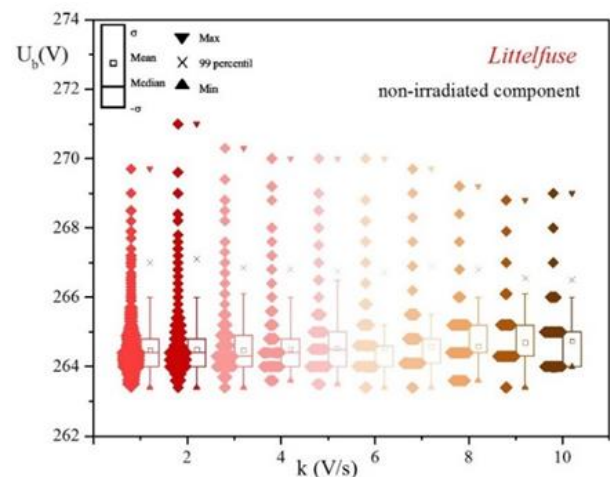


Figure 2: The statistical distribution of breakdown voltage U_b as a function of the voltage increase rate k for the non-irradiated Littelfuse component.

The close agreement between the mean and median values, together with the relatively small standard deviations, confirms the consistency of the measurement procedure. At higher voltage increase rates, the number of distinct breakdown voltage values decreases, resulting in partial overlap of the median with the extreme values. A similar conclusion can be drawn for the components exposed to radiation. As an example, the results for the gas

discharge tube manufactured by Littelfuse are presented in Fig. 3.

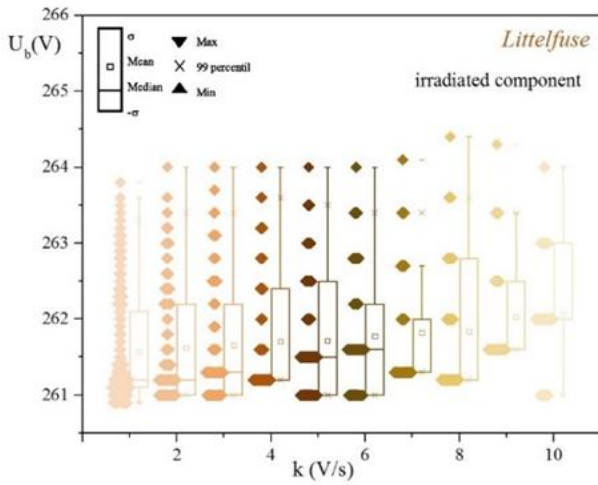


Figure 3: The statistical distribution of breakdown voltage U_b as a function of the voltage increase rate k for the irradiated Littelfuse component.

Fig. 4 illustrates the breakdown voltage distributions for non-irradiated and gamma-irradiated gas discharge surge arresters across three distinct voltage rise rates ($k = 2, 5$ and 8 V/s).

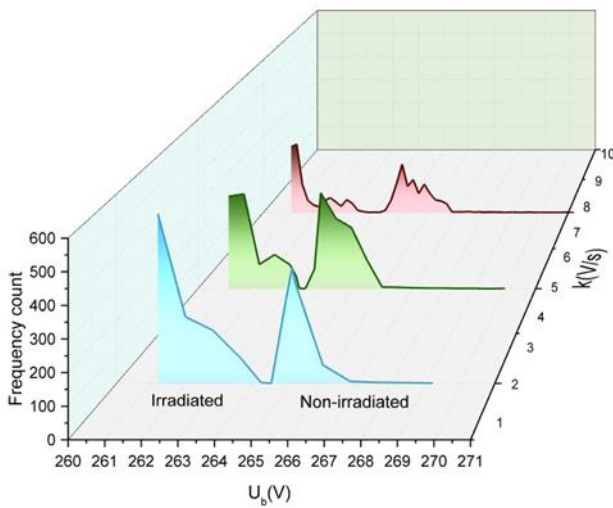


Figure 4: Frequency count of dynamic breakdown voltage U_b for three different voltage rates for the non-irradiated and irradiated Littelfuse GFSA.

The results demonstrate a clear influence of ionizing radiation on the statistical characteristics of breakdown in the gas gap. Under irradiation, the breakdown distributions exhibit

sharper and more pronounced peaks, indicating more localized and reproducible breakdown behavior. This can be attributed to the increased availability of primary electrons generated by ionizing radiation, which facilitates electron avalanche initiation and reduces the statistical delay time before breakdown.

With increasing voltage rate, the distributions become broader and may exhibit additional minor peaks, reflecting greater dispersion in breakdown conditions. Nevertheless, the irradiated condition maintains a more defined statistical response, indicating that ionizing radiation improves the predictability and repeatability of breakdown initiation by reducing the stochastic component associated with initiating electrons.

Overall, the obtained results demonstrate that the dynamic method enables accurate estimation of the static breakdown voltage. In addition, the applied statistical analysis confirms the high repeatability of the measurements and clearly reveals the influence of gamma irradiation on the breakdown characteristics of the investigated gas-filled surge arresters.

3 Weibull Distribution Analysis

To further investigate the statistical characteristics of the breakdown process, the measured breakdown voltage data were analyzed using the cumulative three-parameter Weibull distribution. Owing to its ability to describe stochastic failure phenomena and reliability characteristics of gas-insulated devices, the Weibull model was selected to evaluate the experimental breakdown voltage distributions.

The cumulative Weibull distribution [10] is defined as

$$F(U_b) = 1 - \exp\left(-(B(U_b - U_a))^d\right), \quad (1)$$

where B is the scale parameter, U_a is the location parameter, and d is the shape parameter.

The experimental cumulative distributions together with the corresponding Weibull fits for the CITEL gas discharge tube in the absence of gamma radiation are presented in Figs. 5–7, while the estimated Weibull parameters for all investigated voltage increase rates are shown in Figs. 8 and 9. The same analysis could be performed for the both investigated gas discharge components, without and under gamma irradiation.

In all cases, the fitted curves closely follow the experimental distributions, demonstrating that the three-parameter Weibull model provides an accurate statistical description of the measured breakdown voltages.

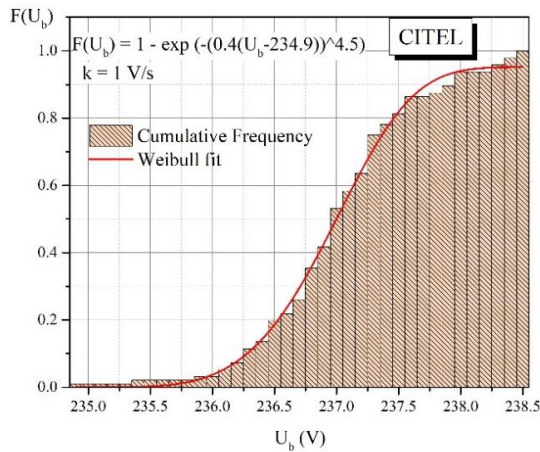


Figure 5: Experimental cumulative distribution and Weibull fit of the static breakdown voltage ($k = 1 \text{ V/s}$).

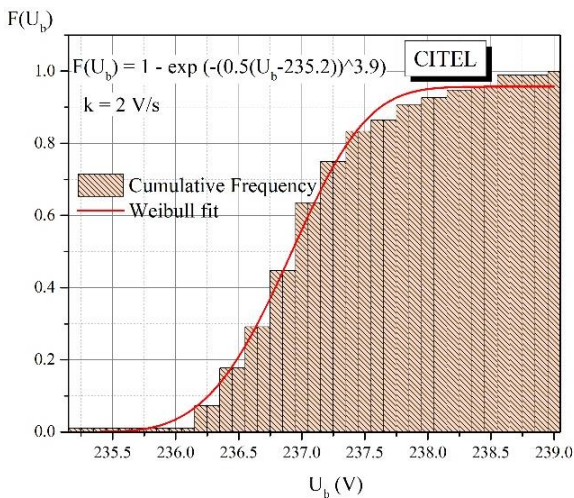


Figure 6: Experimental cumulative distribution and Weibull fit of the static breakdown voltage ($k = 2 \text{ V/s}$).

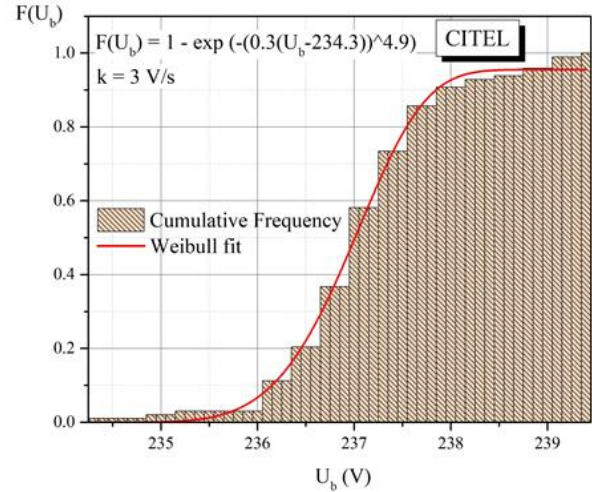


Figure 7: Experimental cumulative distribution and Weibull fit of the static breakdown voltage ($k = 3 \text{ V/s}$).

The obtained Weibull parameters provide additional insight into the breakdown characteristics. The location parameter U_a exhibits only minor variations with the voltage increase rate and remains close to the previously estimated static breakdown voltage (see Fig. 8). This agreement confirms the consistency of the two independent estimation procedures and suggests that U_a can also be used as an indicator of the intrinsic breakdown threshold of the gas-filled surge arrester (The relative deviation is approximately 1.4 %).

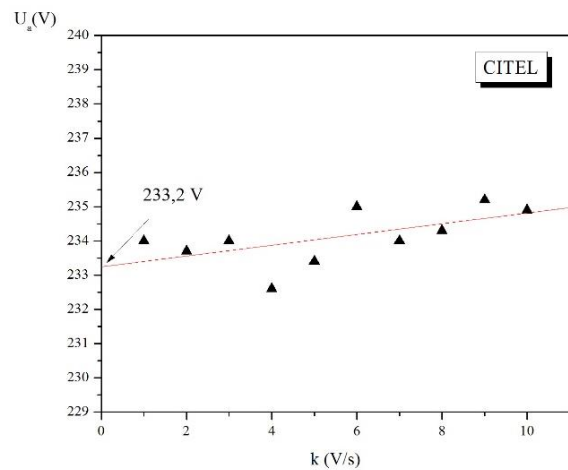


Figure 8: Location parameter as a function of voltage increase rate.

The scale parameter B shows only slight changes over the investigated operating conditions, whereas the shape parameter d proves to be the most informative parameter

for describing the statistical behavior of the breakdown process (see Fig. 9). Since d determines the steepness of the cumulative distribution, higher values correspond to lower statistical dispersion and improved breakdown voltage stability.

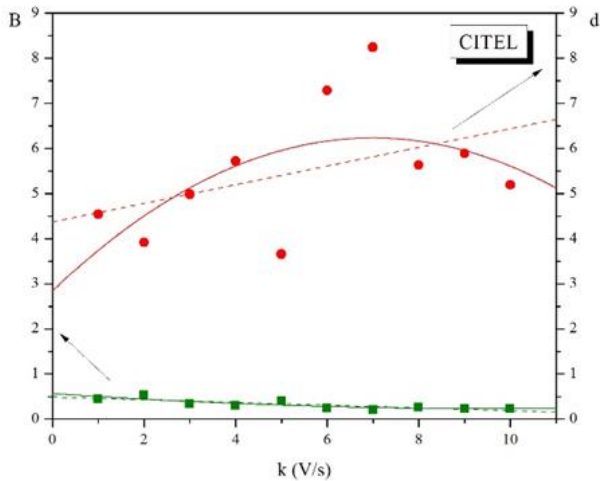


Figure 9: Scale parameter and shape parameter as a function of voltage increase rate.

A comparison of the Weibull parameters obtained before and after irradiation shows that gamma radiation primarily affects the statistical variability of the breakdown process rather than its fundamental mechanism. Although irradiation slightly modifies the distribution parameters, the experimental data remain well described by the same Weibull model.

The fitting quality was evaluated using the coefficient of determination R^2 and the Pearson χ^2 goodness-of-fit test. For all cases, $R^2 > 0.99$, indicating excellent agreement between the experimental and fitted Weibull distributions, while the Pearson χ^2 test confirmed no statistically significant deviation from the model.

Overall, the three-parameter Weibull distribution accurately describes the breakdown voltage of both investigated gas-filled surge arrester types, before and after gamma irradiation. Thus, the Weibull-based approach provides a reliable basis for comparing breakdown characteristics and assessing GFSAs reliability under different environmental conditions.

4 Conclusions

The obtained results confirm the stochastic nature of breakdown voltage in gas-filled surge arresters and highlight the importance of statistical analysis for reliable characterization of their breakdown behavior. The combination of the dynamic method and the three-parameter Weibull distribution provides an effective and reliable approach for evaluating breakdown parameters and assessing the influence of gamma irradiation. The results demonstrate that gamma radiation affects the statistical characteristics of the breakdown process, while the experimental data remain well described by the Weibull model. This confirms that the proposed methodology can be used for reliable comparison of different surge arrester technologies under various operating and environmental conditions.

Future work will include the investigation of additional GFSAs types and environmental influences, as well as the application of advanced data analysis methods, including artificial intelligence based approaches, to support the interpretation of experimental results and further optimize the measurement procedure.

5 Acknowledgments

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SENSORS AND MEMS

Fluidic platform for electrochemical detection of pesticides in water

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We report the processing and performance testing of a miniature analytical sensor platform (ASP) for electrochemical detection of environmental pollutants under flow conditions. The ASP was fabricated from low-temperature co-fired ceramic using multilayer ceramic technology. The cavity was designed to accommodate disposable electrochemical sensors (ES) and enable fluid flow controlled by an external syringe pump. The in-house manufactured ES, with electrical connections, and counter electrodes made from platinum, reference electrode Ag/AgCl, and a graphite-based working electrode (WE), are all integrated on alumina, screen-printed, and fired at temperatures up to 1000 °C in controlled atmospheres.

Finite element modelling software COMSOL Multiphysics was used to evaluate analyte flow in the ASP with different cavity heights, from 2.3 mm to 0.7 mm. Based on the Navier-Stokes equation, we predict the velocity of the fluid in the cavity across flow rates up to 5 ml/min. The model was validated by measuring the cyclic voltammetry response of ES in a well-characterized redox system, potassium ferrocyanide/potassium ferricyanide (HCF), at various flow rates. With a comprehensive understanding of analyte mass transport in both stagnant and flow conditions, we discuss optimal measurement parameters in the ASP for detecting the hazardous pollutant imidacloprid (IMD), a neonicotinoid insecticide frequently found in water and bee-based products.

The current–voltage characteristics of IMD show a single cathodic peak at -1.4 V, consistent with an irreversible electrochemical process. Experimental data demonstrate comparable electrochemical responses of IMD using graphite-based WE under stagnant conditions, in conventional electrochemical cells, and in the ASP, validating the accuracy of measurements in the ASP. The limit of detection (LOD) for IMD, determined by differential pulse voltammetry, was improved by accumulating IMD at the surface of the WE. In stagnant conditions without accumulation, the LOD was $1.1\text{ }\mu\text{M}$, and decreased significantly to 40 nM after 3 minutes of accumulation at a flow rate of 1 ml/min . Continuous electrochemical detection in flow-based systems is appropriate for real-time, in situ monitoring of pollutants in remote environments.

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Experimental Study of Cross-Regime Gas Transport Through Long Microcapillaries: Towards Reliable Predictive Models for MEMS

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In Micro-Electro-Mechanical Systems (MEMS), gas transport differs significantly from conventional macro-scale fluid dynamics because the characteristic dimensions of the system become comparable to the mean free path of gas molecules. Prediction of gas transport becomes increasingly difficult when changes in pressure and capillary diameter induce transitions between different flow regimes. Under such conditions, the flow evolves from continuum and slip-flow regimes toward transitional and free molecular flow regimes, where classical continuum descriptions lose validity [1–5].

Models describing mass transport through microcapillaries have been extensively studied for individual flow regimes, while unified and interpolated models for rarefied microflows have also been proposed [6,7]. However, in practical systems, local variations of the Knudsen number along the capillary can lead to coexistence of multiple flow regimes within a single channel, making reliable prediction of gas throughput increasingly challenging.

In this work, gas flow through long microcapillaries (0.8–1.3 m) with diameters ranging from 2 to 200 μm is experimentally investigated under pressure conditions between approximately 1 and 100 kPa. Experimentally measured throughput values are compared with continuum, slip-corrected, transition-regime, and molecular-flow models in order to evaluate their validity under varying rarefaction conditions.

The aim of this work is to contribute to the development of more reliable predictive models for gas transport in micro-scale systems relevant to MEMS, vacuum microelectronics, semiconductor gas delivery technologies, and controlled gas dosing into vacuum environments.

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Label-free Hela Cells detection

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Abstract: Today, cancer research focuses on characterising the kinetics and state of cancer cells by detecting oncogenic signalling. Label-free optical techniques offer promising non-invasive, high-speed, high-resolution, and straightforward detection of cellular signals. Here, we present a method for detecting signals from non-immobilised HeLa cells in response to a blue LED pulse at a specific frequency, using an a-Si:H p-i-n photodiode and a c-Si photodiode. Results indicate that HeLa cells exhibit a specific, measurable response within milliseconds. The transient response of the a-Si:H p-i-n photodiode makes it a more suitable transducer, given the fundamental defect kinetics in the a-Si:H material. The characteristic, very-low-level, time-varying light response of HeLa cells is attributed to intracellular chemiluminescence (CL) arising from the reaction between nitric oxide (NO) and hydrogen peroxide (H₂O₂). The presented method offers a viable solution for label-free, real-time cell recognition using blue light as a non-destructive reactant, applicable in a sensor array.

Keywords: a-Si:H photodiode; transient response; Hela cells light emission; biosensors; label-free detection; instantaneous lifetime

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1 Introduction

Cancer research needs the development of novel label-free methods for single-cell analysis [1]. The advantage of label-free biosensors is that they enable the direct detection of the selected analyte without chemical modification of the target molecule [2]. Label-free optical biosensors for the direct detection of target DNA mutations employ surface-immobilised DNA probes [3]. In the context of emerging developments in detecting oncogenic signalling, cancer research today focuses on studying the kinetics and state of cancer cells [4].

Label-free optical techniques [5, 6] provide promising non-invasive, high-speed, high-resolution, real-time, highly sensitive, and straightforward detection of cellular signals. In

recent years, microarrays and miniaturised analytical devices have been developed and integrated into lab-on-a-chip (LOC) systems [7-9] using a-Si:H as a transducer. In particular, optical techniques for detecting bioluminescence and chemiluminescence (CL) [8, 9], which detect photons emitted by chemical reactions, are used in life sciences research to monitor and measure biological processes and entities.

The new approach by Kawaguchi et al. [10] for high-efficiency, minimally invasive cancer treatment using label-free blue LED light at 470 nm may exert antitumour effects without damaging normal cells. Their study demonstrated that blue LED light induced intracellular reactive oxygen species (ROS) in sarcoma

cells. All sarcoma cells irradiated with the blue LED showed enhanced green fluorescence compared with the control group. They also investigated the mechanism of sarcoma cell death induced by blue LED irradiation.

Hence, label-free, blue LED light-scattering-based detection of live cells at low concentrations, applicable in microfluidic LoC [8, 9] and in interferometric image scanning microscopy (iISM) [11], is a contact-free technique that maintains cell viability and minimises phototoxicity, and is therefore highly desirable for live-cell studies.

In our previous experiments [12], we observed that the time (t) dependence of the photocurrent, $I_{ph}(t)$, of an a-Si:H p-i-n photodiode over many decades exhibits complex photocurrent dynamics, which have been attributed to the distribution of shallow defects responsible for carrier trapping and release during secondary light generation from the chemiluminescence reaction in HeLa cells.

The present work considers the implementation of the instantaneous lifetime, proposed by Goldie [13], within the previously investigated [12] method for detecting photo-induced chemiluminescence (PICL) signals from non-immobilised HeLa cells in response to blue LED pulses at a specific frequency, and measured using a-Si:H p-i-n photodiodes and a c-Si photodiode under low-bias illumination and low-bias voltage.

The results were compared with those obtained by fitting the measured data with sums of exponential functions using the model of Fehr et al. [14], as proposed by J. Melskens et al. [15], and with the classical model previously used in [16].

After a brief description of the developed method, materials used, and proposed experimental details in Section 2, the obtained results and discussions are presented in Section 3. Finally, the conclusions are given.

2 Materials and Methods

2.1 Measurement set-up

The HeLa human cell line (cervical carcinoma) culture is described in detail elsewhere in [12]. A blue LED (RGB LED Lamp, Kingbright, China) emitting at a peak wavelength of 430 nm was used as a pulsed monochromatic excitation light source. The commercial c-Si p-i-n photodiode, Osram BPW 21, was used as a control photodiode positioned laterally to the analyte. HeLa cells in the cell culture medium (CCM) were placed without immobilisation using a pipette onto the microscope slide and manually aligned on the a-Si:H photodiode surface. The measurement set-up was placed in a dark metallic box. The preparation of HeLa cells in the cell culture medium (CCM) is described in more detail in our previously published paper [12].

The a-Si:H photodiode was connected in series with a load resistor, R_L , of 10 k Ω , a DC power supply (Keysight Power Supply E36313A, Malaysia USA), and a digital multimeter (DMM, Keysight 6 1/2 Digital Multimeter Truevolt 34461A). The current and voltage were measured using the DMM (Keysight 6 1/2 Digital Multimeter Truevolt 34461A). All instruments were connected to the PC, and the simultaneous measurement process was automated using test flow sequences created in Keysight BenchVue. Here, we will focus on the measured transient responses, particularly those of a-Si:H photodiodes.

2.2 The transient response measurements

A function generator (Keysight Function Generator 35510B, USA) was used to drive a pulsed blue LED light source. A pulsed signal with a frequency of 333 Hz and an amplitude of 4 V was applied. The DC voltage (Keysight Power Supply E36313A, USA) was -2 V. A step voltage was applied to the blue LED, and the transient response of the photodiodes below (a-Si:H) and lateral (a-Si:H, c-Si) to the analyte,

placed in a dark metallic box, was captured with an oscilloscope (Keysight DSOX2014A Infini Vision 4CH 100 MHz 2 Gsa/s, USA). The details of the long-time transient conduction and transient response measurements are described elsewhere in [12] and our previously published papers.

3 Theoretical Models

The well-known defect pool model [17] describes the density of states (DOS) in the mobility (energy) gap of amorphous silicon, responsible for trapping–detrapping events and recombination processes, and for the gap-state parameters [18, 19] that influence changes in the local electric field and control the PD photocurrent as it decays over time [20]. It is well known that at lower frequencies, recombination occurs through centres of the $D^{+/0}$ and $D^{0/-}$ levels of normal silicon dangling bonds. Recombination through the recombination centres of the $D^{0/-}$ level dominates at low frequencies.

The initial steady-state photocurrent [13, 20] may be expressed in a-Si:H, as

$$I_{ph}(0) = qAG\mu\tau\bar{\xi} \quad (1)$$

where q is the fundamental electronic charge, A the photodiode's cross-sectional area for current flow, G the carrier generation rate, and the applied electric field $\bar{\xi} = U/d_i$ in the depleted intrinsic photodiode i-layer of width d_i , μ the mobility of free charge carrier electrons, and τ the lifetime of the free charge carriers.

Assuming emission from the deep traps, all weak bonds below the thermalisation energy E_{th} , neglecting in the initial approximation the barrier lowering in the case of electron accumulation, have been entirely converted to the defects. The energy an electron needs to overcome the barrier for the forward reaction rate depends on the time t it attempts to escape

$$t = \nu_0^{-1} e^{E_{th}/kT} \quad (2)$$

where $\nu_0 = 10^{12} s^{-1}$ is the attempt-to-escape frequency, E_{th} is the trap activation energy or

trap depth, k is Boltzmann's constant, and T is the absolute temperature. The photocurrent depends directly on the mobility-lifetime product, $\mu\tau$. Knowing the lifetime τ , we can determine the energies of metastable dangling bonds (MDBs) that contribute to photocurrent transients during the CL reaction in HeLa cells.

To estimate the trap-limited lifetime, τ , three approaches were applied to the measured $i_{ph}(t)$ curves. The photocurrent rise and decay over time intervals were fitted using the model of Fehr et al., an exponential function with a square time dependence in the exponent [14], proposed by [15], and the model used in [16], a superposition of two exponentials, as previously described in [12]. The analysis is now extended to the instantaneous lifetime proposed by Goldie, obtained from the entire growth and recovery period, such that

$$\tau(t) = - \frac{1}{n_{free}(t)} \frac{dn_{free}(t)}{dt} \quad (3)$$

where $n_{free}(t)$ is the time-free electron concentration, permitting a spectrum of lifetime values to be generated.

4 Results and discussion

In our experiment, HeLa cells in CCM solution and CCM were illuminated with blue LED light at a critical frequency of 333 Hz, incident on the p-side of the PDs. The time evolution of the measured transient photovoltage/photocurrent responses of the a-Si:H p-i-n PD1 below the analyte is shown in Figure 1, and those of PD2 and PD3, positioned laterally relative to the analyte, are shown in Figures 2 and 3, respectively. Illuminating the HeLa cells with pulsed blue LED light, we identified the “resonance frequency” at which the a-Si:H p-i-n photodiode exhibits overshoot (Fig. 1). Simultaneously, smaller second peaks emerge in the c-Si photodiode transient response. After the light switch-off, the PD below the analyte shows a larger shoulder. Further, we established that after one hour of illumination of

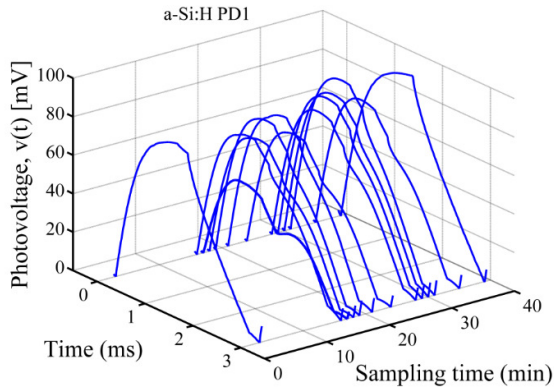


Figure 1: Time evolution of the transient response of an a-Si:H p-i-n photodiode (PD1) placed below the analyte.

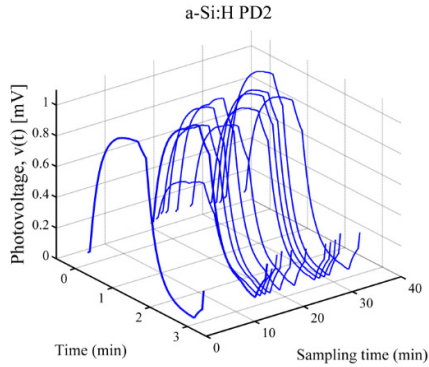


Figure 2: Time evolution of the transient response of an a-Si:H p-i-n photodiode (PD2) placed lateral to the analyte.

HeLa cells with blue LED light of 430 nm, the cells are no more active. The detailed description of deviations in photocurrent/photovoltage transient responses is provided in depth in [12]. The measured curve shape and magnitude change over time follow the activity of HeLa cells (CL signal) and consequently the occupancy of the metastable defects in a-Si:H.

The amplitude of the first peak of the c-Si PD3 varies over time following HeLa cell activity (CL). The second peak (Fig. 3 no. 2) is a response to the CL process and to light emission from HeLa cells.

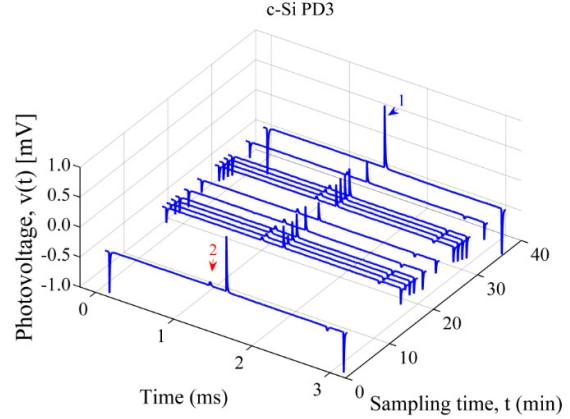


Figure 3: Time evolution of the transient response of an c-Si p-i-n photodiode (PD3) placed lateral to the analyte.

Figure 4 shows the calculated defect activation energies, given by Eq. (2), derived from measured a) on- and b) off-transient responses of photodiode PD1 with a HeLa cell in CCM on the surface, at a 17 min sampling time after the start of illumination. The blue curve shows the calculated energies according to the instantaneous lifetime proposed by Goldie [13]. The red squares represent on obtained by fitting to the measured curve to a linear and a quasi-linear exponential function with one time constant; the green triangles by fitting to a two-exponential function; and the magenta triangles by fitting to the Fehr exponential function with square time dependence in the exponent.

We can deduce that the instantaneous lifetime/energy is quasi-constant during the CL reaction. The lifetime calculated by fitting the measured curve to linear and two-term exponential curves over- and under-estimates the instantaneous lifetime. The one obtained by fitting to the Fehr exponential function shows smaller deviations. The magnitude of the error here depends on the number of points used in fitting.

The instantaneous lifetimes/energies, calculated from the measured photovoltage response recorded at 17 min and 24 min after the start of illumination (Fig.5), show that the

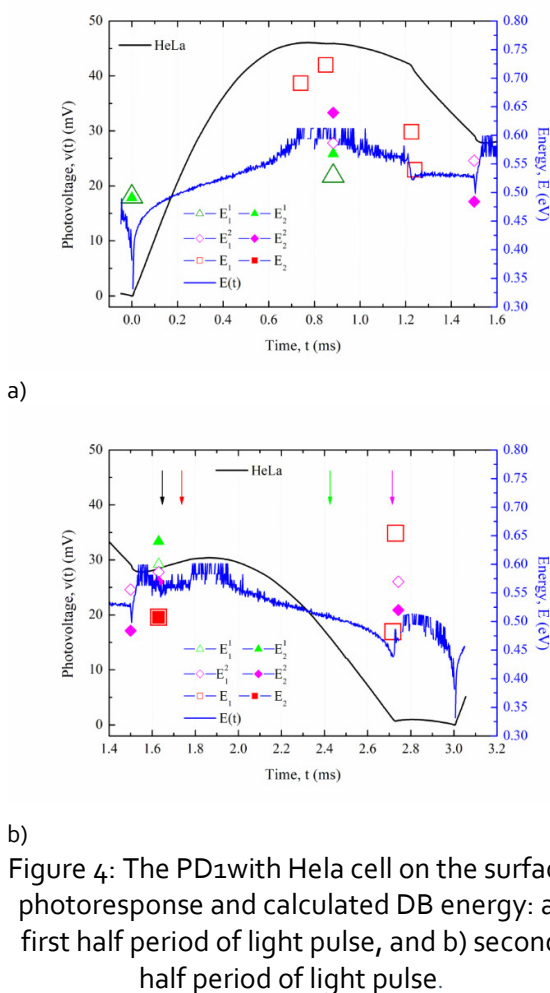


Figure 4: The PD1 with HeLa cell on the surface photoresponse and calculated DB energy: a) first half period of light pulse, and b) second half period of light pulse.

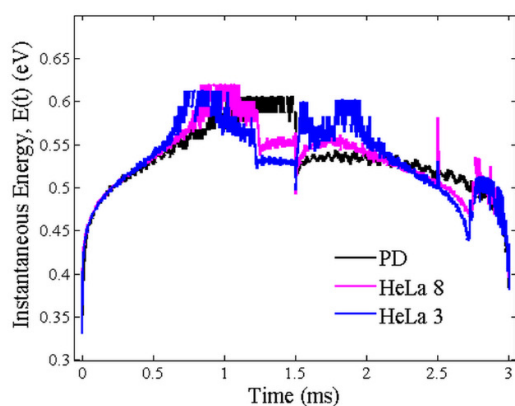


Figure 5: The calculated energy, E from the instantaneous lifetime, $\tau(t)$ proposed by Goldie, for photodiode PD1 and photodiode PD1 with HeLa cells in CCM on the active surface at the 3rd and 8th sampling times after the start of consecutive photocurrent response measurement.

beginning of the CL reaction changes over time and duration. Also, for PD, the lifetime drops sharply to a lower value at light switch-off, whereas in the HeLa CL reaction the decline is almost linear and is visible before the light is switched off. This is consistent with the well-known fact that the CL is a linear process, because the intensity of the emitted light is linearly proportional to the concentration of the analyte [21], in our case, HeLa cells emitting light.

5 Conclusions

We demonstrated detection of HeLa light emission arising from their intrinsic chemiluminescence, excited by blue LED light. The calculated instantaneous lifetime more precisely delineates the onset and duration of the CL reaction than the measured photocurrent transient response of an a-Si:H p-i-n PD with analyte. The presented method offers a viable solution for label-free, real-time cell recognition using blue light as a non-destructive reactant, applicable in a sensor array.

6 Acknowledgments

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Thermal Optimization of a DNA Amplification in a Micro-PCR System

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Rapid molecular diagnostics are essential for effective point-of-care (POC) infectious disease management [1]. While microfluidic thermocyclers offer a path toward "Extreme PCR" [2], achieving laboratory-grade precision at sub-second transition speeds remains a significant engineering challenge. This work presents the thermal and metrological characterization and optimization of a microfabricated PCR platform utilizing a four-tether titanium-on-silicon architecture (modified structure from [3]). We demonstrate ultra-fast heating ramp rates of 175 °C/s enabling seamless transitions between denaturation 95 °C and annealing 60 °C plateaus.

A primary focus of this study is the characterization of the chamber optimization and system dynamics ([4], [5]). Experimental results show that the micro-PCR with a 500 nL sample, mineral oil encapsulation, and PDMS-glass chamber increases yield and reproducibility of the DNA amplification in comparison to silanized virtual chamber.

We developed a PID control loop integrated into an STM32. This algorithm includes optimization for silanized virtual chamber and PDMS-glass chamber, so that it reaches the set temperature with lowest possible swing and in an optimal time.

Furthermore, we investigated the thermal damping stability of the Micro thermocycler. The system robustness was verified through 40 continuous cycles of a three-step PCR protocol, showing zero sensor drift (Figure 1) or mechanical degradation. This characterization provides a robust framework for the design of high-speed, reliable POC diagnostic devices where thermal speed must be balanced with biological safety.

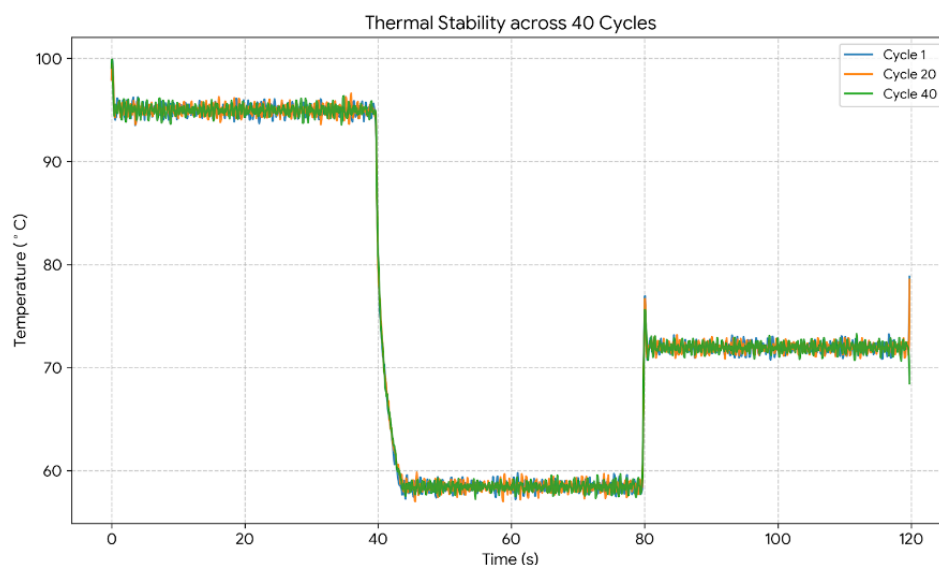


Figure 1: Thermal stability of the system across 40 cycles.

The platform performance was characterized with biologically relevant conditions specifically investigating the impact of different microfluidic chamber surface treatments—including a silanized virtual chamber, a PDMS-glass chamber, and a PDMS-glass chamber passivated with BSA—alongside the addition of 1 μL BSA directly to the sample. The thermal cycling protocol consisted of an initial denaturation step at 95 °C for 5 minutes, followed by 40 cycles of denaturation at 95 °C for 40 seconds, annealing at 60 °C for 40 seconds, and extension at 72 °C for 40 seconds.

The DNA amplification performance varied significantly across the tested microfluidic chamber configurations, highlighting the impact of surface interactions and vapor containment on PCR efficiency (Figure 2):

- **Silanized Virtual Chamber (V₁, blue circles):** Demonstrated the poorest performance, exhibiting the delayed quantification cycle ($C_q \approx 33$) and lowest overall yield during early-to-mid cycles. This inhibition was primarily driven by incomplete oil coverage over the virtual chamber, which allowed partial evaporation of the 500 nL sample during thermal cycling. Evaporation leads to localized ionic strength shifts and reagent depletion, severely delaying amplification.
- **Native PDMS-Glass Chamber (V₂, orange squares):** Achieved earlier amplification ($C_q \approx 13$) than V₁, as the solid chamber enclosure and levelled mineral oil coverage prevented sample evaporation. However, performance remained suboptimal compared to V₃ due to non-specific adsorption of *Taq* DNA polymerase onto the hydrophobic PDMS and glass channel walls. This surface binding reduces the effective concentration of free enzyme in the reaction volume.
- **BSA-Passivated Glass + 1 μL BSA Sample Additive (V₃, green triangles):** Exhibited the highest amplification efficiency and earliest C_q (≈ 9), reaching peak endpoint fluorescence

(~ 11.6). The combination of static chamber passivation and dynamic BSA supplementation effectively blocked non-specific binding sites on the microchannel walls, preventing *Taq* polymerase adsorption and maintaining optimal enzyme kinetics.

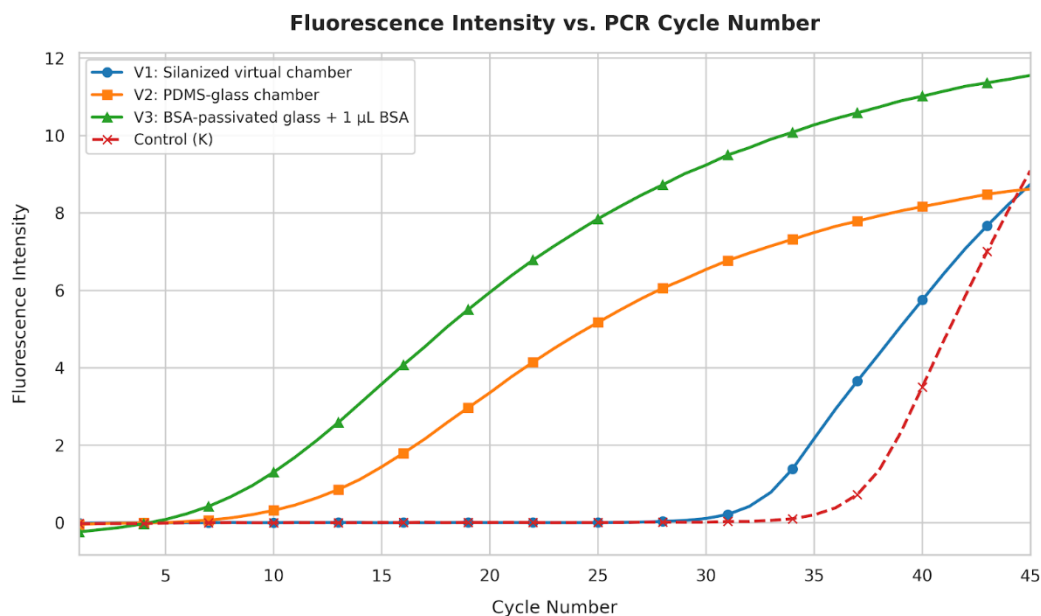


Figure 2: PCR fluorescence intensity plotted against cycle number for a 500 nL sample volume across four experimental conditions: a silanized virtual chamber (V1, blue circles), a native PDMS-glass chamber (V2, orange squares), a BSA-passivated PDMS-glass chamber with 1 µL BSA added directly to the sample (V3, green triangles), and a control sample (K, red dashed line/crosses).

These findings demonstrate that balancing high-speed thermal control with combined static and dynamic BSA passivation provides a robust framework for reliable, ultra-fast micro-PCR diagnostic devices.

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Nanostructuring of Boron-Doped Diamond for Electrochemical, Sensing, and Environmental Applications

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Boron-doped diamond (BDD) combines a wide electrochemical potential window, low background current, high chemical and mechanical stability, and resistance to corrosion and fouling, making it an attractive electrode material for electroanalysis, sensing, photoelectrochemistry, energy storage, and advanced water treatment. Conventional planar BDD electrodes, however, are often limited by low electrochemically active surface area and mass-transfer characteristics. This work summarizes how micro-, nano-, hierarchical, and three-dimensional structuring can tailor BDD functionality for specific electrochemical applications.

BDD thin films were deposited by LA MWCVD on planar and microstructured Si, microstructured Al₂O₃, and porous Al₂O₃ substrates. Additional nanoscale modification was achieved by plasma etching, producing high-aspect-ratio BDD nanostructures. The resulting electrodes ranged from planar 2D systems to microstructured, hierarchically micro/nanostructured, and macroporous 3D flow-through architectures. Their morphology, electrochemically active surface area, charge-transfer behaviour, potential window, and application-oriented performance were evaluated by SEM, Raman spectroscopy, cyclic voltammetry, electrochemical impedance spectroscopy, and electrochemical experiments.

For environmental applications, structured 2D and porous 3D BDD electrodes enabled efficient electrochemical oxidation of persistent organic pollutants [1]. A 3D flow-through BDD architecture supported the degradation of Direct Red 80 with reduced energy demand, while planar and microstructured electrodes achieved rapid removal of diclofenac [2]. LC-HRMS analysis further showed that electrode morphology and current density influence not only removal efficiency but also the distribution of degradation and transformation products.

In this article, BDD nanostructuring is demonstrated not only as an effective strategy for increasing the electrochemically active surface area, but also as a versatile tool for engineering the electrode-electrolyte interface and tuning electrochemical functionality.

Results and Discussion

The electrochemical properties of BDD depend not only on boron concentration and diamond quality but also on surface architecture. Micro-pyramidal Si and microstructured Al₂O₃ substrates provide micrometre-scale topography, plasma etching creates nanoscale features in the BDD layer, and porous ceramic substrates enable the transition from conventional 2D electrodes to macroscopic 3D flow-through systems. In the Direct Red 80 study, combined Si and diamond structuring increased the real surface area by up to 34.4%, whereas porous flow-through BDD electrodes exhibited electrochemically active surface areas up to 45.5 cm², compared with approximately 6–7 cm² for planar electrodes.

Structuring is also relevant for sensing, photoelectrochemistry, and energy storage, where rapid heterogeneous electron transfer, large accessible area, and a wide potential window are required. Microstructured $\text{Al}_2\text{O}_3/\text{BDD}$ improved electron-transfer characteristics and active area. In $\text{Si}/\text{BDD}/\text{TiO}_2$ photoelectrodes, oxygen-plasma etching produced BDD nanotip-like features of approximately 150 nm height and 50 nm thickness, increasing photocurrent about 4.5 times compared with unstructured BDD/TiO_2 and 6.5 times compared with ITO/TiO_2 . Nanostructured BUNCD on Si micro-pyramids also reduced impedance and reached a maximum specific capacitance of 53.7 mF cm^{-2} at 2.54 mA cm^{-2} [3].

For environmental electrochemistry, scaling BDD into a 3D flow-through geometry enhanced pollutant-electrode interaction and mass transport. Direct Red 80 treatment achieved more than 95% decolorization within 60 min with an energy consumption of approximately 5.9 kWh m^{-3} . Diclofenac removal exceeded 99% in NaCl electrolyte with an energy consumption of 1.8 kWh m^{-3} . Overall, multiscale BDD structuring provides a general electrode-design strategy for stable sensors, photoelectrodes, energy-storage components, and low-energy reactors for advanced wastewater treatment.

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Electrochemical Screen-Printed Electrode-Based Sensor For Ergosterol Detection As A Marker Of Potential Food Fungal Contamination

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Fungal contamination remains a major concern in food safety, creating a demand for rapid and cost-effective analytical tools suitable for routine screening. Mainly mycotoxins, produced by certain fungi, are the most risky fungal products leading to severe poisoning [1].

Ergosterol (provitamin D₂, ergosta-5,7,22-trien-3 β -ol) is the main sterol of fungal cell membranes, where perform functions comparable to cholesterol in animal cells. Ergosterol is responsible for membrane fluidity, permeability, and structural integrity [2]. These functions are closely related to ergosterol concentration in membrane. It is also present in animal cells, where it serves as one of the precursors for vitamin D. Several studies have confirmed that ergosterol levels correlate with the fungal growth and can therefore serve as an indicator of potential fungal contamination in food [3,4].

The aim of this work was to investigate the applicability of developed screen-printed boron-doped diamond electrodes (SP-BDDEs) for the electrochemical determination of ergosterol using square-wave voltammetry. Owing to their wide potential window, low background current and disposable format, SP-BDDEs represent a promising platform for rapid electrochemical screening. In contrast to conventional chromatographic techniques [5], the proposed approach offers the potential for simple, portable and cost-effective analysis.

The applicability of the electrochemical platform was evaluated using ergosterol standard solutions, fungal mycelia and artificially contaminated food samples, including bread and grain. Sample preparation involved alkaline saponification followed by liquid-liquid extraction. Since sample preparation significantly affects electrochemical response, particular attention was paid to optimization of the extraction procedure. The developed method enabled reliable electrochemical detection of ergosterol with a linear response within the investigated concentration range. Optimization of the extraction protocol improved ergosterol recovery from approximately 20% to nearly 50%, demonstrating the importance of sample preparation for sensitive electrochemical determination.

These preliminary results confirmed the applicability of SP-BDDEs for ergosterol detection and demonstrate their potential as an electrochemical platform for rapid screening of fungal contamination in food matrices. Ongoing work is focused on reduction of matrix effects and validation of the method using real food samples.

Acknowledgment

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Practical Aspects in Electroanalysis with Screen-Printed Sensors with Boron-Doped Diamond Electrode

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Nowadays, a wide variety of electrochemical sensors are manufactured for the analysis of various compounds. In addition to bulky disc electrodes of classical design made of, e.g., glassy carbon or metals, there are numerous miniaturized sensors incorporating a complete three-electrode setup. Several manufacturing technologies are commonly used to prepare these sensors, which aim to be low-cost, mass-producible, and easy to operate while still delivering sufficient electroanalytical performance [1]. Such devices are primarily designed as disposable, low-cost, one-shot sensors that allow simple measurements in the field or enable undemanding point-of-care testing.

In the case of screen-printed sensors, the materials used, conditions, and technological operations at each layer-forming step must not affect the resulting electrochemical performance of the prepared working electrode. Most screen-printed sensors use low-temperature-curable graphite inks of various compositions to form working and auxiliary electrodes. The composition of the ink greatly influences the electrochemical behavior of the working electrode. It is usually a tradeoff between the properties important for printing and good electrochemical characteristics.

The reference part is also important for the proper function of the screen-printed sensor. Generally, simple and easy-to-prepare pseudoreference systems made of silver or silver/silver chloride inks are used. However, such configurations are strongly influenced by the presence of chloride ions in the solution, leading to changes in the reference electrode potential and subsequent shifts of voltammetric signals along the potential axis. Furthermore, some analytes may react with or bind to silver at the reference part, also causing a potential shift, which will be documented in the case of simultaneous electrochemical oxidation of uric acid, guanine, and adenine.

Boron-doped diamond has been used as a promising material for working electrodes, exhibiting a wide potential window, chemical inertness, low background currents, improved fouling resistance, and long-term electrochemical stability. Recently, planar sensors with boron-doped diamond working and auxiliary electrodes prepared by chemical vapor deposition on the same substrate with a screen-printed silver reference electrode were developed. To improve the stability of the reference, silver was electrolytically coated with AgCl [2]. Although primarily intended for single-use, these sensors showed improved durability even in organic solvents such as ethanol and acetonitrile. This enables, for example, the electrochemical detection of organic compounds in spices, with performance comparable to that of a glassy carbon electrode. Moreover, repetitive measurements and quantification using a single sensor are possible, especially for analytes that do not adsorb on the working electrode surface. This was confirmed, e.g., in the electroanalysis of nicotine and methylxanthine alkaloids, such as caffeine [3], theobromine [4], and theophylline [5],

where there was no visible deterioration of the electrode surface even after a hundred voltammetric scans. On the contrary, screen-printed sensors with a graphite working electrode modified with multi-walled carbon nanotubes and a silver pseudoreference electrode were less stable and unsuitable for the analysis of highly acidic beverage samples, where the reference part can deteriorate quickly.

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STUDENT SESSION

Development of an LCR meter

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Abstract: This paper presents the development of an LCR meter in the frequency range from 1 KHz to 100 KHz. First, the principles of operation are presented and then the design is discussed. Important construction, firmware, and software development choices are also highlighted. The device is later used to measure the parameters of multiple components across a frequency range. The results are later compared to a commercial LCR meter. In the final part, possible improvements are presented.

Keywords: LCR meter; FFT; anti-aliasing filter; analog-to-digital converter

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1 Introduction

When designing electronic circuits, I often found myself needing to know the properties of basic elements, most important being inductance, capacitance, and resistance. The latter two usually did not pose a problem as most commercial multimeters feature resistance and capacitance measurement modes. The inductance measurement, however, was quite problematic as dedicated measurement instruments are less common and usually more expensive. Despite being possible, measurements with other instruments were time-consuming, so I decided to build my own instrument to measure all of them in a single step.

2 Theory of operation

To measure the impedance, I decided to measure the voltage and current over the measured component to which an excitation signal was applied. To convert the current to a voltage, which could be measured with an analog-to-digital converter (ADC), I chose a

transimpedance amplifier (TIA), which offers multiple benefits over an ordinary resistor [1].

The voltage and current signals first pass through an analog frontend and are sampled by the ADC. They are then processed digitally to extract the amplitude and phase information.

To do that, a fast Fourier transform (FFT) algorithm is used to transfer the signal from the time domain to the frequency domain, from which the amplitude and phase are calculated.

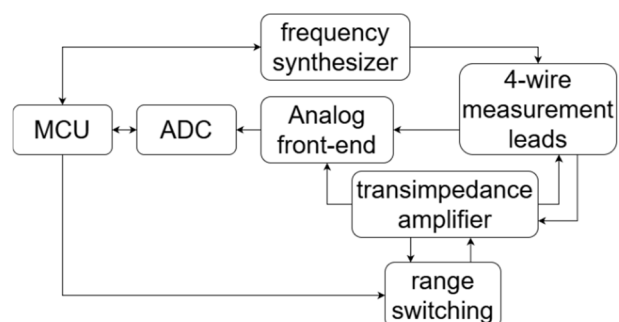


Figure 1: Instrument block diagram

To improve the accuracy of the instrument and decrease the influence of the measurement leads, a 4-wire (Kelvin) measurement method was chosen.

The block diagram of the instrument is shown in the Figure 1.

2.1 Previous attempt

In the initial version of the instrument, the amplitude measurement was made using resettable peak detectors to reduce the needed sampling rate of the ADC. This method achieved an accuracy of $\pm 20\%$.

It was also slow, as measurements took more than 100 ms due to the time needed for the peak detector to reach the final value.

I attempted to measure the phase shift between the current and voltage signals using the internal counter peripheral of the microcontroller (MCU) to measure the delay.

This method proved to be unsuitable due to noise present in the signals. Therefore, for this purpose, a different measurement method using FFT was chosen.

3 Development

3.1 Requirements

The instrument was designed with a goal of measurement frequencies from 1 KHz up to 100 KHz, which set some constraints on the design; however cost-effectiveness was also a large factor in the component selection process.

3.2 Component selection

The most important part, which dictated the design, was the ADC. I selected the MCP33131-10-E/MS, which uses the successive approximation register (SAR) technique, has a resolution of 16 bits, and a sampling frequency of 1 MHz, which gave some headroom with the anti-aliasing filter design.

For the digital processing of signals, I chose a microcontroller (MCU) as opposed to a field-programmable gate array (FPGA), as I was already familiar with them. The MCU used is the STM32H723ZG, which offers up to six serial peripheral interface (SPI) ports and 24 timer peripherals [2], which allow for communication with external circuitry. It also offers many general-purpose input output (GPIO) pins and four direct memory access (DMA) units [2]. These are used to offload the ADC sampling from the processor.

For the frequency synthesizer, I chose the AD9837BCPZ-RL7 due to its sufficient operating frequency and simple to use SPI interface.

Because its datasheet [3] does not mention the maximum current load, I added an output buffer, the BUF634A, which can deliver 250 mA [4]. This is sufficient to drive a $100\ \Omega$ load at the maximum voltage of 10 V as seen in Eq. (1).

$$I_{max} = \frac{U_{max}}{R} = \frac{10\ V}{100\ \Omega} = 100\ mA \quad (1)$$

The chosen anti-aliasing filter topology was an active 8th order Butterworth lowpass filter, made from four cascaded voltage-controlled voltage-source (VCVS) filters shown in Fig. 1 [5].

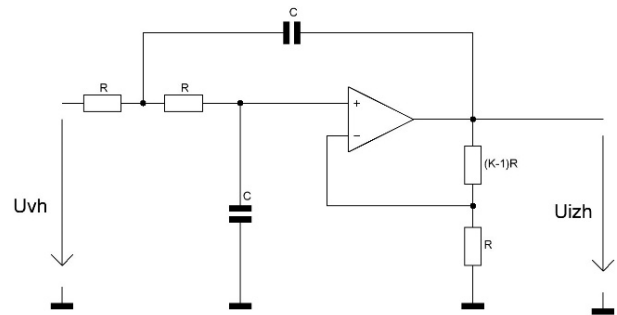


Figure 2: single stage VCVS filter

The cutoff frequency was selected at 100 KHz by choosing appropriate values of R and C based on Eq. (2) [5]:

$$f_c = \frac{1}{2\pi RC} \quad (2)$$

The chosen values were:

- $R = 3.3\ K\Omega$
- $C = 470\ pF$

By using Eq. (2), we get a cutoff frequency at:

$$f_c = \frac{1}{2\pi \cdot 3.3 \text{ k}\Omega \cdot 470 \text{ pF}} = 102614 \text{ Hz} \quad (2)$$

The gain values (K) were chosen based on the following table which gives the response of a Butterworth filter [5]:

Table 1

n	1	2	3	4
K	1.038	1.337	1.889	2.610

Given the value K, a suitable resistor value was chosen based on Eq. (3) [5]:

$$R_n = R(K_n - 1) \quad (3)$$

The table below shows the chosen resistor values:

Table 2

R	R ₁	R ₂	R ₃	R ₄
Value	120 Ω	1.1 K Ω	3 K Ω	5.1 K Ω

For the operational amplifier I opted for the OPA4172 due to its low noise and high enough slew rate of 10 V/ μ s, yielding a result as shown in Eq. (4).

$$SR_{min} = 2\pi f U_m = 2\pi \cdot 100 \text{ KHz} \cdot 10 \text{ V} = 6.28 \frac{\text{V}}{\mu\text{s}} \quad (4)$$

3.3 Simulation

To verify the filter performed as expected before building it, I simulated the design in LTSpice.

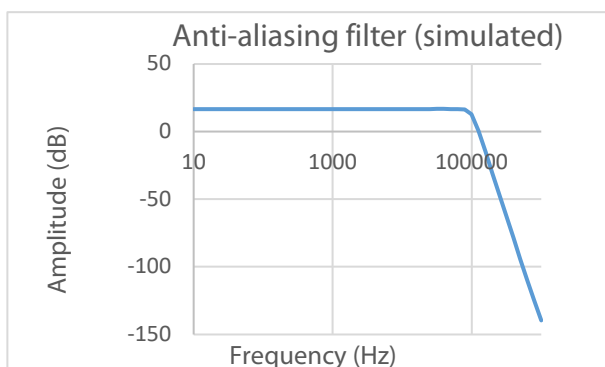


Figure 3: Amplitude frequency response of the anti-aliasing filter (simulated)

The simulated response in Fig. 2 shows the filter operates correctly. Its -3 dB point, however, was lower than expected, being around

94 KHz. This was likely due to the input capacitance of the chosen operational amplifier.

4 Construction

To quickly prototype the design, I used the NUCLEO-H723ZG MCU development board which integrates the STM32H723ZG together with a debugger.

The analog front-end design was split into multiple functional blocks which could be fabricated separately as to allow individual testing. The blocks were later connected to a prototyping board.

To power the device, I used a switching power supply, the RT-65C from the manufacturer Mean well. It provides +15 V and -15 V used to power the analogue circuitry, as well as +5 V used to power the MCU development board.

I designed a printed circuit board (PCB) which incorporates a MCU, buttons, and a liquid crystal display which was used to set measurement parameters and show the results.

I also made an enclosure using 3D-printed parts and sheet metal.

The figure below shows the constructed device.



Figure 4: Constructed device

5 Firmware and software

The firmware was written in C, using the STM32Cube integrated development environment (IDE) while the initialization code was generated by the STM32CubeMX application.

5.1 Interfacing the ADC

The ADC uses an SPI interface, where the chip select pin also starts the conversion process. To generate a fixed sampling rate, the internal timer peripheral was used as a PWM generator with a frequency of 800 kHz, which is lower than the maximum sampling frequency of the ADC (1 MHz). This was necessary as the construction prohibited the use of the maximum clock speed.

To reduce the number of GPIOs used, and guarantee simultaneous sampling, the same timer pin was used for both ADCs.

The DMA peripheral was used to periodically transmit data on the SPI bus, which operated in a full-duplex master mode. This activated the SPI clock and caused the ADC to transmit the readings.

Another DMA stream was also used to transfer the received data from the SPI to the FFT buffer.

The same configuration was applied to two DMA units, each moving data from its dedicated SPI interface to the FFT buffer.

5.2 Fast Fourier transform

I decided to use a library to calculate the FFT, specifically the CMSIS DSP library, which supports real FFT lengths of up to 4096 samples [6] when using 32-bit floating point representation.

To obtain measurements for the frequencies between frequency bins, I used the average of three bins, namely the one closest to the selected measurement frequency and the bin above and below.

This spectral averaging improves frequency estimation at the cost of slight amplitude smoothing near sharp response transitions.

5.3 Range switching

As the TIA has a selectable feedback resistor, a method was needed to determine its value. I chose an approach where the impedance is

first measured and then compared with the selected measurement resistor. If the measured impedance (without calibration) is within a range specified by Eq. (5), the measurement is considered complete:

$$R_n \cdot 0.3 < |Z| \leq 7 \cdot R_n \quad (5)$$

In the case the value falls outside of the calculated range, the program switches to a lower or higher valued resistor, according to the magnitude of the impedance.

The measurement is repeated until a suitable resistor is found or cannot be changed to a more appropriate value (e.g. at minimum or maximum range).

5.4 Calibration

As the instrument includes circuits, which have a variable amplitude and phase response with respect to frequency, I decided to perform the calibration at multiple frequencies, specifically at each frequency corresponding to the FFT output.

Calibration was not performed for the first output of the FFT, as it represents the DC offset. Outputs above 100 KHz were also excluded, as they are outside the measurement frequency range.

Calibration values were stored on an external SPI-connected memory (EEPROM).

To calibrate a frequency point, a calibration component is connected between the measurement leads. Its impedance is then measured and stored. The next time a measurement at the same frequency point is performed, the measured impedance is divided by the previously stored impedance and multiplied by the true value of the calibration component, as shown in Eq. (6).

$$Z = \frac{Z_x}{Z_{cal}} \cdot Z_{com} \quad (6)$$

In the equation above, we have the following variables:

- Z – corrected impedance,
- Z_x – measured impedance,
- Z_{cal} – measured impedance of the calibration component,

- Z_{com} – true impedance of the calibration component.

As all impedances are measured as complex values, this procedure calibrates both amplitude and phase.

This method, however, requires a component with a constant frequency amplitude and phase response.

As I did not have such a component, I used a 100 Ω laboratory calibration resistor which only exhibited an impedance change of 0.371 Ω and phase angle change of 2.52° across the 1 kHz to 100 kHz frequency range.

As resistors of higher values had larger phase and impedance variations across the frequency range, I decided to only calibrate the 100 Ω measurement range.

This did not account for the non-constant response of other feedback resistors used in the TIA; it only corrected the frequency responses of the connected circuitry.

5.5 Software

To add frequency sweep capabilities to the device, I decided to use the debuggers virtual communication port (VCP) capability to communicate with a personal computer (PC).

The PC was running a Python script which would set the measurement frequency, perform the measurements and display them in a plot.

To display the plots, I used the library Matplotlib, while Openpyxl was used to store the results in an Excel file.

6 Measurement results

I evaluated the filter frequency response and accuracy of the measurements.

6.1 Filter frequency response

To verify the anti-aliasing filter is operating correctly I measured its frequency response

using an oscilloscope and a function generator.

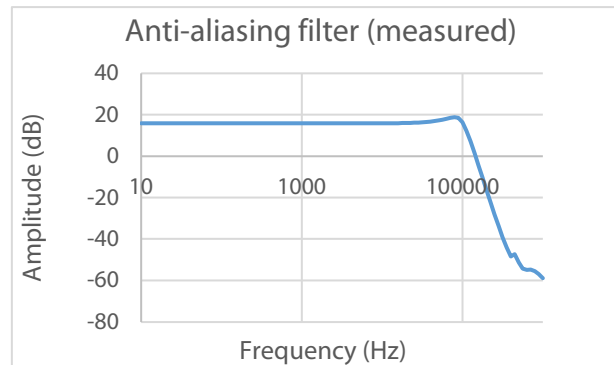


Figure 5: Amplitude frequency response of the anti-aliasing filter (measured)

The results shown in Fig. 5 confirmed the filter operated as expected.

6.2 Accuracy measurements

To estimate the accuracy of the device, I compared it to a commercial LCR meter (GW-Instek LCR-8220) with a specified basic accuracy of $\pm 0.08\%$ [7].

I measured the impedance and phase shift of a capacitor (100 nF), inductor (10 mH), and resistor (10 k Ω), across the entire frequency range of the constructed device (1 kHz – 100 kHz) with both instruments.

The sweep function of the commercial LCR meter measures across the selected frequency range at 267 points [8], while the Python script used for sweeping the frequency range on the constructed instrument allows only integer values for the steps per decade parameter.

This prohibits the use of an odd number of sample points for two decades of frequency change. So, in order to estimate the values at the frequency points of the commercial instrument, I measured over 268 frequency points and subsequently applied the linear interpolation on the constructed instrument data set.

To calculate the relative measurement error, I used Eq. (7) for the impedance and Eq. (8) for the phase:

$$\Delta Z_r = \frac{(Z - Z_c) \cdot 100\%}{Z} \quad (7)$$

- Z – impedance measured with LCR-8220
- Z_c – impedance measured with the constructed instrument

$$\Delta \varphi_r = \frac{(\varphi - \varphi_c) \cdot 100\%}{\varphi} \quad (8)$$

- φ – phase angle measured with LCR-8220
- φ_c – phase angle measured with the constructed instrument

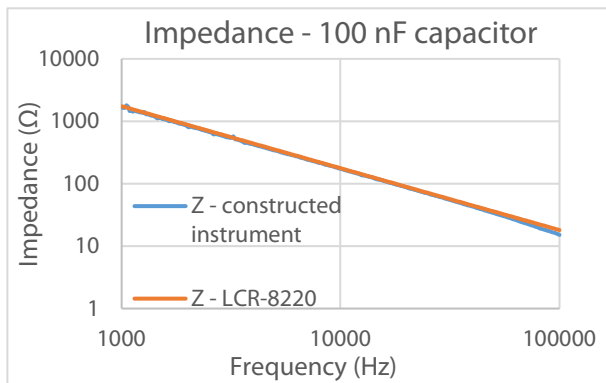


Figure 6: Impedance - 100 nF capacitor

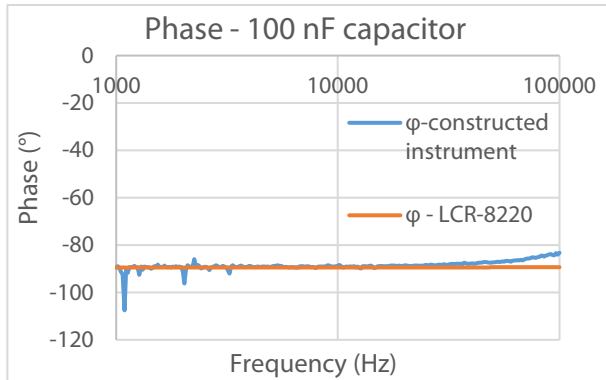


Figure 7: Phase - 100 nF capacitor

As seen in see Fig. 6 and Fig. 7, the measurements of the capacitor on the constructed instrument differ most from the LCR-8220 measurements at frequencies close to the lower and higher limit of the measurement frequency range.

At lower frequencies, more noise is present, while at higher frequencies a gradual increase in the measurement error occurs.

The measured capacitor was a standard THT ceramic capacitor.

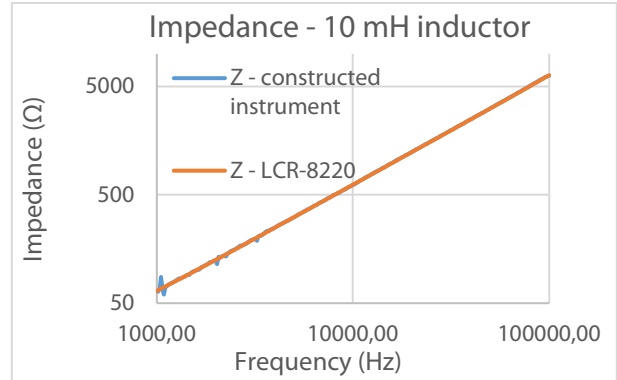


Figure 8: Impedance - 10 mH inductor

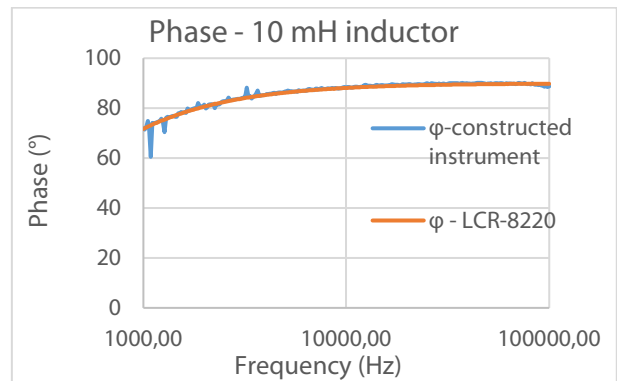


Figure 9: Phase - 10 mH inductor

In the inductor measurements on Fig. 8 and Fig. 9, noise can also be seen at lower frequencies. In Figure 99 we can also see a gradual increase in measurement error.

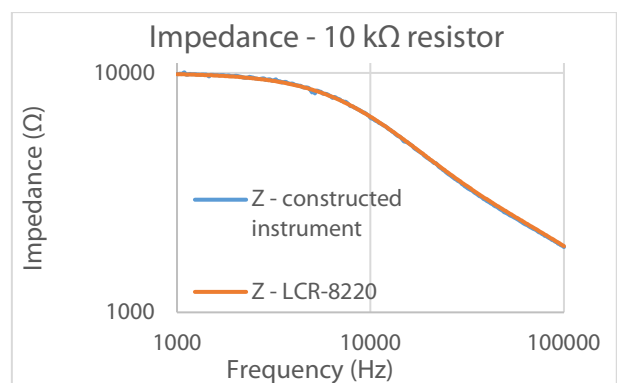


Figure 10: Impedance - 10 kΩ resistor

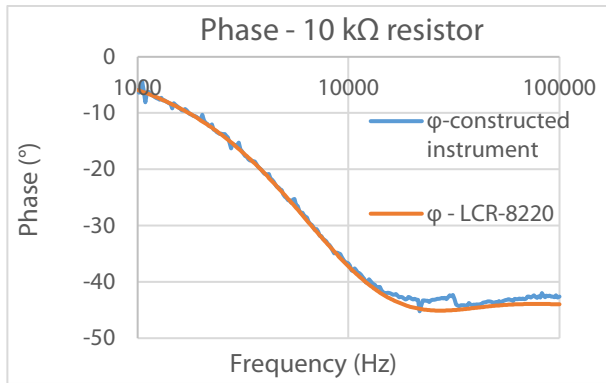


Figure 11: Phase - 10 k Ω resistor

In Fig. 10 and Fig. 11, the noise is also present in the lower frequencies. Also, in Figure 11 an increasing error can be observed starting from 10 KHz peaking at 5.93 % before decreasing toward an average of 2.2 %.

An increase in error can also be seen near the upper frequency limit.

The maximum impedance measurement difference between the instruments was ± 27.55 %, which, when added to the accuracy of the LCR-8220, gives a final accuracy of ± 27.63 %. The highest phase difference was ± 29.86 %, which gives a final phase accuracy of ± 29.94 %.

7 Possible improvements

The most important improvement would be to upgrade the ADC resolution and sample rate. This would improve the resolution and decrease the noise of the system.

With higher frequency components being used in other parts of the instrument such as filters, higher measurement frequencies could also be accommodated.

An increase in ADC bit depth and sampling rate would also increase the strain on MCU resources, so moving to an FPGA platform would be sensible as it would also increase its DSP capabilities.

To further increase the signal-to-noise ratio (SNR), a larger FFT data set could also be used. A larger data set was not used in this iteration due to lack of a support for larger buffers in

the selected library and due to memory limitations.

To accommodate lower measurement frequencies a dynamic ADC sampling rate could be implemented, which would set a constant ratio between measurement and sampling frequency in order to ensure enough full waves would be stored in the FFT buffer. This would also require an anti-aliasing filter with programmable bandwidth on the input.

A possible improvement to the calibration procedure would be to replace the constant component value in Eq. 6 with a stored value, measured using a more accurate LCR meter.

Calibration could then be performed on all measurement ranges without the need for calibration components with a constant frequency response.

8 Conclusions

The constructed instrument achieved an accuracy of less than ± 30 %. While this leaves a lot of room for improvement, it confirmed the viability of the chosen approach using FFT to calculate magnitude and phase.

The designed anti-aliasing filter performed as expected by the calculations and simulation.

The addition of a PCB used for displaying the readings, combined with a custom enclosure allowed the device to function as a standalone instrument without the need for a PC connection.

9 Acknowledgments

I would like to thank both mentors for their help throughout this project.

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Designing a High-End PCB in Kicad

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Abstract: Modern stage lighting installations increasingly rely on addressable RGB and RGBW fixtures, whose channel counts exceed the practical limits of the DMX512-A standard. This paper describes the hardware design and implementation of a six-layer Art-Net and sACN controller designed in KiCad, an open-source electronic design automation (EDA) suite. The controller combines an STM32H743 microcontroller, an integrated three-port Ethernet switch, and four high-speed pixel output stages capable of driving up to fifty DMX universes simultaneously. Particular attention is given to controlled-impedance routing, electromagnetic interference (EMI) mitigation, and thermal management, all of which were necessary to guarantee reliable operation in the demanding electrical environment of touring and architectural lighting rigs. The completed board was validated against its design targets and is presented together with a discussion of KiCad's suitability as a professional EDA platform.

Keywords: DMX512; Art-Net; STM32; LED lighting; pixel mapping

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1 Introduction

Addressable RGB and RGBW LED fixtures require individual control over every pixel. The traditional DMX512-A standard sends data over RS-485 cables at 250 kbps, carrying up to 512 channels per universe [1]. This capacity is only enough for about 170 RGB pixels. Controlling large LED setups with DMX requires running dozens of separate cables, which increases cost, creates signal delays, and causes wiring clutter.

Ethernet-based protocols like Art-Net and sACN (E1.31) solve this issue by sending thousands of DMX universes over standard network cables [2]. This shifts the work to the receiving controller, which must quickly turn network packets into precise timing signals for the LED pixels without stuttering or crashing.

This paper details the hardware design of a custom DMX/Art-Net controller created in KiCad. The board receives network data over Ethernet and outputs control signals to four independent LED pixel ports. Key focus areas include stackup design for a six-layer circuit board, careful trace routing for high-speed signals, and heat management.

2 Design Concept and Target Specifications

Instead of using a simple and low-cost microcontroller, that could struggle under heavy network loads, this project uses STMicroelectronics' STM32H743VGHx, which is known for its speed, reliability and wide industrial applications.

The controller handles Ethernet networking and LED timing simultaneously in separate

processing areas so that high network activity does not interrupt lighting playback.

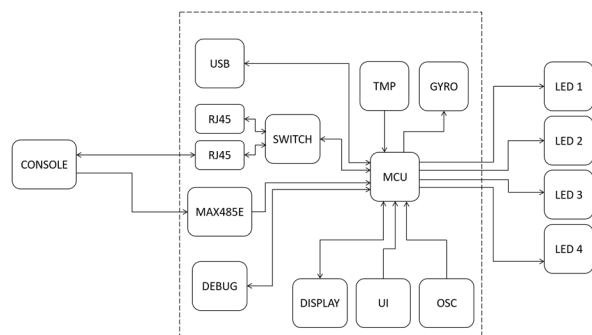


Figure 1: Block diagram

The block diagram of the device is shown in Figure 1, while key specifications are summarized in Table 1.

Table 1: Device highlights

Parameter	Specification
Protocol support	Art-Net, sACN (ANSI E1.31), DMX512-A, RDM (ANSI E1.20), GDTF
Universe capacity	Up to 50 concurrent DMX universes, corresponding to approximately 8,500 RGB or 5,100 RGBWW pixels across four output ports
Pixel protocol compatibility	Native support for over 75 SPI-based pixel protocols, including WS2811, WS2812B, APA102, SK6812, and UCS1903
Frame synchronisation	Hardware-level support for MADRIX 5 Sync, ArtSync, and sACN Sync
Power input	Dual-input architecture (USB-C or 24 V DC) with automatic switchover
Onboard sensing	Ambient temperature, humidity, and orientation sensing

3 Development Platform: KiCad

Designing a multi-layer, high-speed circuit board requires capable software. The schematic and layout for this board were created entirely in KiCad.

We opted for developing in KiCad since its license places no limitations on its use, board size, or component count, and supports up to 32 copper layers. It is also the software we have been using in school.

KiCad's parametric impedance calculator and native DRC rules were used to enforce 50 Ω single-ended and 100 Ω differential targets during layout. The 3D viewer aided early clearance checks against the extruded aluminum enclosure.

4 Hardware Architecture

We opted for a slightly complex design, since we wanted to have a product, free of additional modules and therefore simple to connect and to use.

4.1 Processing Core

An STM32H743VGHx is a microcontroller based on an ARM Cortex-M7 core running at up to 480 MHz. It manages the core operations of the board. It features 2 MB of dual-bank flash memory, 1 MB of SRAM, a ChromART graphics accelerator, and multiple independent DMA channels. [3]

4.2 Power Management and Distribution

Power is supplied through a TPS2116DRL power multiplexer. It switches automatically between the USB-C interface and the main external 24 V DC input without causing voltage dips or unwanted microcontroller resets [4].

An LMR60420 synchronous buck converter subsequently steps the incoming 24 V rail down to the logic-level voltages while maintaining low output ripple and low switching noise [5].

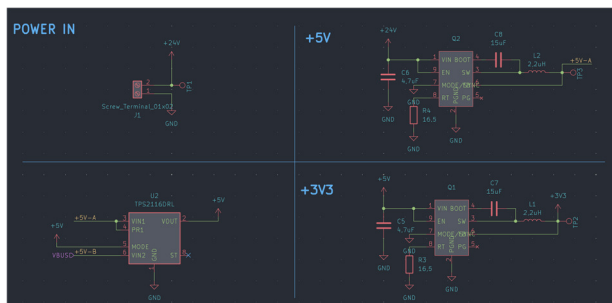


Figure 2: Power scheme

4.3 Physical Interfaces and Environmental Sensors

DMX512-A and RDM signalling are handled by a MAX485E RS-485 transceiver, chosen for its enhanced electrostatic discharge (ESD) protection against ground-loop voltage spikes, a common hazard in touring installations.

Local configuration and status reporting are provided by a 1.5-inch, 240×240-pixel TFT/OLED display paired with hardware buttons. The user interface allows on-site IP configuration and menu navigation.

An onboard LIS3DH accelerometer automatically reorients the display according to the mounting position, while an HDC1080 sensor continuously monitors internal temperature and humidity to track enclosure conditions.

4.4 Integrated Ethernet Switch

A common single point of failure in standard pixel nodes is their reliance on an external network switch mounted near the lighting truss.

To remove this dependency, an unmanaged three-port Ethernet switch, the Microchip LAN9303, was integrated directly onto the PCB. Two of its ports are routed to shielded RJ45 or ruggedised Neutrik etherCON connectors for daisy-chain pass-through wiring, while the third port connects internally, via an MII/RMII interface, to the MAC controller of the STM32H743 processor.

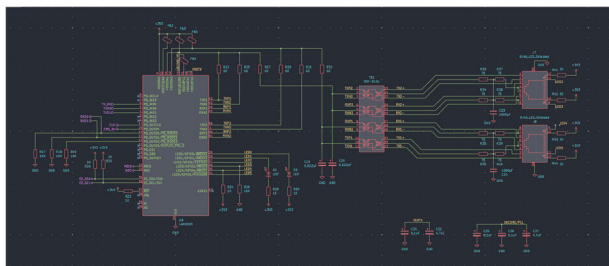


Figure 3: Switch scheme

This arrangement offers three architectural/networking advantages:

First, it eliminates the need for individual home-run cabling from a central rack switch to every fixture, since nodes can instead be linked sequentially along the structural truss.

Second, because the LAN9303 forwards pass-through frames at the hardware layer, downstream nodes receive synchronisation frames with minimal propagation delay.

Third, the switch circuitry operates on an isolated power domain, remaining active during microcontroller resets or firmware updates, so that downstream nodes in the chain do not drop offline.

5 Six-Layer PCB Design and Signal Integrity

Routing high-speed digital buses immediately adjacent to high-current LED power traces within a compact footprint required a carefully optimised stackup.

Table 3: Layers and functions

Layer	Function
1 Top signal	High-speed routing, including Ethernet MDI differential pairs, MCU clock lines, and memory buses; hosts the MCU, filtering networks, and connectors
2 Ground plane	Solid, unbroken copper pour directly beneath Layer 1, providing a short return path and minimising loop inductance
3 Inner signal	Lower-speed control lines, I ² C/SPI sensor buses, and display signalling, shielded between ground and power planes
4 Power plane	Split copper zones for 3.3 V, 5 V, and 24 V rails, isolating switching noise from the high-speed digital layers

5 Ground plane	Second solid ground pour, mirroring Layer 2 to maintain symmetric impedance for Layer 6 traces
6 Bottom signal/power	Auxiliary routing, supplemental ground fill, structural mounting pads, and high-current power distribution

A six-layer topology, summarised in Table 3, was selected to balance signal integrity, low-impedance power distribution, and thermal dissipation.

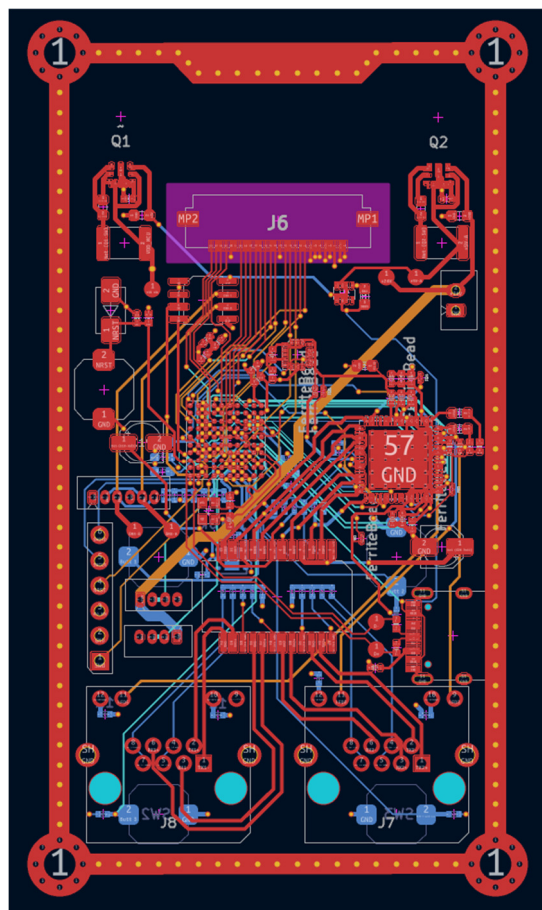


Figure 4: Layout:

At a microcontroller core frequency of 480 MHz and Ethernet clock rates of 100 MHz, PCB traces behave as transmission lines rather than simple conductors, and incorrect trace geometry can introduce impedance mismatches, reflections, ringing, and data corruption.

Trace impedance depends on trace width, copper thickness, the dielectric height above the reference plane, and the permittivity of the FR-4 substrate.

The Ethernet MDI traces leading to the LAN9303 were designed for a differential impedance of $100\ \Omega \pm 10\%$, using appropriate trace width and separation gaps.

The gaps were calculated using KiCad's built-in transmission-line calculator; clock distribution lines and SPI buses were matched to a single-ended target impedance of $50\ \Omega$.

Several layout rules were applied consistently across the high-speed sections of the board. The MDI+ and MDI- traces were length-matched to within 0.1 mm using serpentine tuning, minimising phase skew and common-mode noise.

All high-speed traces were routed continuously over a solid reference plane on the adjacent layer, avoiding any crossing of plane splits or voids, which is a common source of EMI radiation.

Vias were avoided on the $100\ \Omega$ differential pairs wherever practicable; where a layer change was unavoidable, adjacent ground-stitching vias were placed to preserve a continuous return-current path.

6 EMI Shielding, Grounding, and Thermal Management

Because the controller operates in close proximity to high-power switching LED drivers and wireless communication equipment, EMI containment was addressed using stitched vias and heat spreading with via matrices.

Copper edge plating around the outer perimeter of the board, tied directly to system ground, suppresses lateral electromagnetic radiation from the inner layers.

Dense arrays of stitching vias along the board boundaries and copper-pour perimeters bond the internal ground planes together,

forming a structural shield around the high-frequency sections.

The RJ45 connectors galvanically isolate the external network cabling from the board's ground plane, further filtering common-mode noise.

On the thermal side, concentrated via matrices were placed directly beneath the LMR60420 buck regulator and the microcontroller, conducting heat into the large internal copper planes.

7 Mechanical Integration

Beyond its electrical requirements, the board layout is constrained by the mechanical profile of its enclosure.

The board outline, mounting holes, and edge clearances were imported directly from the mechanical CAD model. This ensured a precise fit within the custom housing.

High- and low-voltage sections are distributed across the opposite sides of the board: Ethernet inputs and DMX XLR connectors along one edge; the display is centered; and the high-current SPI LED output terminals along the opposite edge.

Trace corners throughout the board use 45-degree bends rather than right angles to further minimize signal reflections. High-contrast silkscreen labelling is applied to speed up manual assembly and field troubleshooting.

8 Results

The prototype six-layer controller successfully demonstrated the performance capabilities of its core processing architecture. Powered by the STM32H743 running at 480 MHz and paired with the LAN9303 Ethernet switch, the board processed up to 50 DMX universes in real time without data loss or timing delay.

During bench validation of the manufactured PCB, an unexpected component failure occurred in the automatic power multiplexer IC (TPS2116DRL).

This hardware failure interrupted intensive long-term stress testing; therefore, these tests remain incomplete at the time of this publication.

Nevertheless, initial functional tests verified that the microcontroller, high-speed routing, network switch, and display subsystems operate as designed.

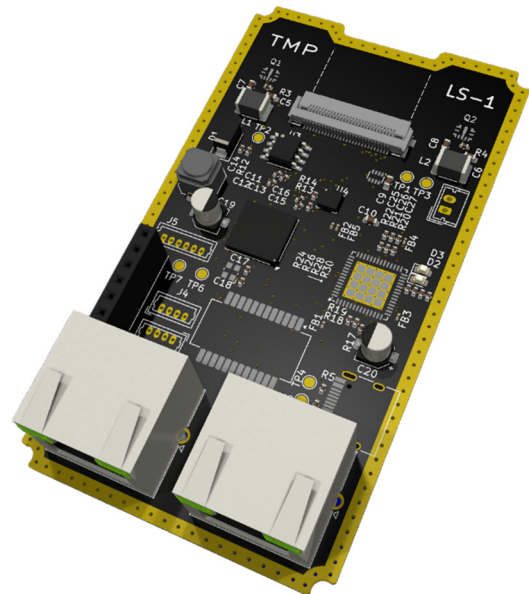


Figure 5: 3D render of PCB

9 Conclusion

This project demonstrates that KiCad is fully capable of handling complex, high-speed, multi-layer PCB designs. Although certain advanced features required manual workarounds during layout, the project met its design goals and specification targets.

Ultimately, KiCad proved to be a reliable EDA tool for this hardware project.

10 Acknowledgments

The author acknowledges Prof. Dr. Patricio Bulić at the Faculty of Computer and Information Science, University of Ljubljana, for his assistance with PCB schematics and valuable insights provided.

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Optimizing Exhaustive Search for the Game of Domineering

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Abstract: Exhaustive solvers for combinatorial games are simple to implement, but their use is limited by the exponential growth of the number of states. This paper examines how far a simple exhaustive solver for the mathematical game of Domineering can be pushed mainly through program-level optimizations, without relying on strong problem-specific observations and reductions.

The problem is initially approached with a simple recursive solver and is later optimized with memoization, bitboard state representation, bitwise move generation, heuristic move ordering, a fixed-size transposition table, and root parallelization. Alongside these optimizations, a more mathematical pruning approach is also tested and compared. The developed solver variants are benchmarked across different hardware configurations and board sizes.

The results show that these optimizations allowed exhaustive search to remain practical for considerably larger board sizes. However, exponential growth remains the main limiting factor, and solving larger boards still requires strong problem-specific observations and reductions.

Keywords: domineering; game theory; optimization techniques; data structures

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1 Introduction

Nowadays many research problems are being tackled with the help of computers since they offer substantial processing power and computational heuristics. Most commonly, solving problems with computers still relies heavily on advanced mathematical reductions and observations since they can often drastically reduce computation time.

This paper focuses on comparing different optimization methods for an initially simple solver for a mathematical game called Domineering.

However, in contrast to most modern solvers, its main goal is not to compute entirely new

results, but instead to see how far a solver relying on almost no mathematical reductions and observations can be pushed.

Through the comparison of different optimization techniques, this paper shows how different aspects of the solver, from speed to memory consumption, are affected.

2 Theoretical Background

In this section, we will briefly present the theoretical background required for understanding the problem and optimizations.

2.1 Game Theory

Game theory is a branch of mathematics focused on analyzing different games and game situations in which players make independent decisions. Players' interdependence causes them to consider the other players' possible decisions while formulating their strategy.

The process of playing a game is typically represented as a state graph consisting of nodes and edges, where nodes represent different game states and edges represent moves that the player whose turn it is can perform.

2.2 Domineering

Domineering is a mathematical game usually played on a rectangular grid. Two players have a collection of dominoes, which they place on the grid in turn, covering up squares. One player places them vertically, while the other places them horizontally. As in most combinatorial games, the first player who cannot move, or in this case, cannot place a domino, loses.

A sample game of Domineering played on a 4×4 board can be seen in Fig. 1. Here, we see the vertical player making the first move and the horizontal player losing in the sixth move.

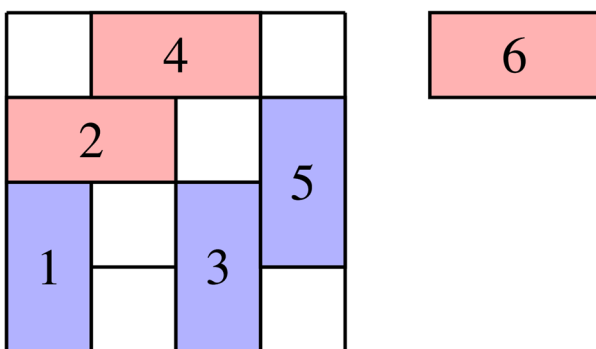


Figure 1: Sample game of Domineering.

The most interesting problem that combinatorial game solvers investigate is who will win the game if both players play optimally.

The largest board for which the outcome is currently known is 11×11 [1]. At that size, the rough upper bound for the number of states is about 2.66×10^{36} . If a program

checked one billion states per second, exhaustive enumeration would take about 84 quintillion years. This is more than six billion times the current age of the universe.

2.3 Big O Notation

Big O notation is a mathematical way to describe an algorithm's time and memory complexity in relation to the input size, denoted by variables such as n . Common examples include:

- $O(1)$ – Constant time
- $O(\log n)$ – Logarithmic time
- $O(n)$ – Linear time
- $O(n \log n)$ – Log-linear time
- $O(2^n)$ – Exponential time

2.4 Basic Algorithm

The algorithm's purpose is to compute which player will win from some starting board. Most commonly, the answer is computed for empty rectangular boards.

The most basic algorithm that can be used is a simple recursive one. From a given state, it will test all the allowed moves one by one.

If a move guaranteeing a win for the player who is currently on the turn is found, the algorithm reports that the current state is a winning state, and if no winning move is found, the algorithm reports that the current state is losing.

Let W denote the board's width and H denote the board's height. Since it doesn't matter who covered the field, we just have to know whether it is covered or not. The upper bound on the number of possible game states is limited to $2^{W \cdot H}$ (some of the states are impossible). Since the basic algorithm will search the entire state graph, its time complexity is $O(2^{W \cdot H} \cdot WH)$. The additional $W \cdot H$ factor comes from iterating over all possible next moves.

3 Optimizing the Algorithm

In this section, we will explain what optimizations can be applied to the basic algorithm to improve its running time.

3.1 Optimizing State Representation

As mentioned before, a state can be represented by encoding whether each field is free or occupied. The most basic data structure allowing this is a simple 2-dimensional array of Boolean values. However, as we quickly notice, there will be a lot of wasted space since a Boolean value requires 8 bits of memory, while it only stores 1 bit.

Since the board dimensions with which the solver will have to deal are at most 11×11 we can use a single integer, with its bits representing the fields of the grid. This will also allow us to use bitwise operations which are well optimized in modern CPU architectures.

3.2 Memoization

Memoization is an optimization technique that stores previously computed states for later use to avoid computing the same thing multiple times.

In the case of the previously described solver, multiple different move sequences may lead to the same board state. Instead of recomputing the answer from scratch when the same state is encountered again, we can just reuse the stored result, saving a lot of compute time.

Writing and accessing the data we want to save can be handled by using a data structure called a hash map. It allows lookup and insertion operations in $O(1)$ while requiring $O(n)$ memory, where n is the number of entries.

An example of using memoization can be seen in Fig. 2. We can see the function calls prevented by memoization shown in gray.

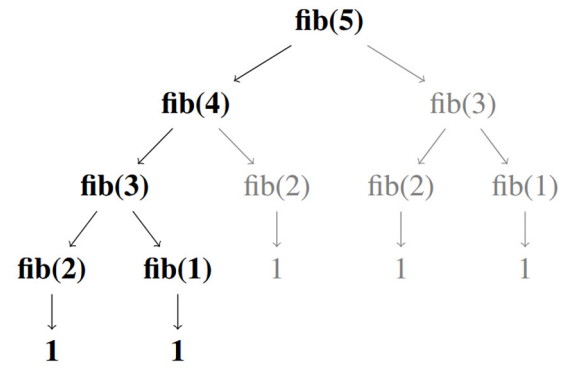


Figure 2: Call tree of a recursive function $fib(N)$ yielding the N^{th} Fibonacci number.

3.3 Bitwise Operations

Up to this point, one of the bigger bottlenecks was the generation of all possible next moves from the current state. Generating moves from a single state requires two loops to check all possible grid placements in $O(W \cdot H)$.

Since bitwise operations on integers are well optimized and run in constant time, we could reduce this step's time complexity to $O(1)$ and, consequently, the whole program's time complexity to $O(2^{W \cdot H})$.

By performing the following operation (1), where *empty* denotes the integer mask representing the empty fields of the current state, we can generate a mask containing only the valid anchors at which the dominoes can be placed on the next move when it is the vertical player's turn.

$$anchors = empty \wedge (empty \gg W) \quad (1)$$

Here, $\wedge$ denotes bitwise AND and $\gg$ denotes a bitwise shift. The shift operation is used to align each empty field with the field one row above it, and the bitwise AND checks whether both fields are free.

A similar combination of bitwise operations can also be used to generate a mask of all the valid moves for the horizontal player.

A representation of the steps taken to achieve the final anchors bitmask, where gray tiles represent binary 0 and white tiles represent binary 1 can be seen in Fig. 3.

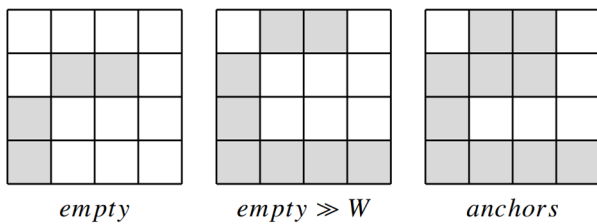


Figure 3: Representation of the steps.

3.4 Move Ordering

Move ordering is a heuristic optimization in which our program first checks the moves that are more likely to yield a winning state.

After some analysis, we notice that winning moves are often located near the center of the board.

To order the possible moves, we first generate them using bitwise operations, and then we sort them by the anchor’s Manhattan distance [3] to the center. The additional time spent ordering the moves is outweighed by the fact that fewer states must be checked.

3.5 Transposition Table

With the previously discussed optimizations, the naive solver could solve boards of size up to 6×6 in reasonable time.

When trying to solve the next size, the solver ran into a new issue of running out of memory because of the linear relation between the hash map’s size and the number of game states visited. This problem can be solved by using a transposition table, whose memory usage is constant.

A transposition table is a data structure that allows us to store results of previously performed searches, like the previously mentioned hash map. It still allows lookup and insertion operations in $O(1)$ while using a constant amount of memory. The memory reduction comes with a massive tradeoff of occasionally having to forget some of the saved results.

Underneath a transposition table is just a simple array. When inserting or accessing state data, a hash value is assigned using Zobrist hashing [2]. That value is used as an index in the array. It is inevitable that two values will eventually map to the same table index. When choosing which value to keep, we use different replacement policies such as keeping the newest value, the one that was computed at the latest stage of the game, or both. Most commonly, multiple transposition tables are used with different replacement policies to achieve better performance.

3.6 Root Parallelization

Root parallelization is a multi-threading technique where multiple independent search trees are built simultaneously from the same root state. The speed of the program scales with the number of threads, but only until one of the running threads finds a solution.

This optimization is especially beneficial on computers with multiple cores, such as modern supercomputers, like the one used for testing.

3.7 Pruning

Even though we decided not to use mathematical optimizations and observations at first, we could not avoid the temptation to optimize it an itsy bitsy tiny bit and see the impact on our solver. We decided to implement a simple observation from the Obsequi solver [4], used to solve a 10×10 board.

4 Comparison

Each version of the solver was tested on two different machines to measure their performance across varying hardware configurations. The following setups were tested:

- Ubuntu Windows Subsystem for Linux (WSL) on Windows 11: Ryzen 9 5900HX with 8 cores and 16 GB of RAM (Razer Blade 14 2021)

- Arnes high-performance computing (HPC) cluster running AlmaLinux OS: AMD EPYC 9254 with 24 cores and 128 GB of RAM

The solver was constrained not to run for more than one hour. In addition, if the program ran out of memory, it would be terminated.

At first glance, the Arnes HPC cluster seemed like it would outperform the other setup.

It turned out that its resources are shared on-demand between multiple users. With the fact that the EPYC CPU cores had lower single-thread performance in comparison to modern desktop and laptop CPU cores, it performed worse unless we were running the multithreaded version of the solver.

The source code for all solver variants and other scripts is available on GitHub [5].

4.1 Results

We compared the execution time (in milliseconds) of the solvers across different board sizes. In single-threaded versions, the Ryzen 9 5900HX significantly outperformed the EPYC 9254 due to its higher single-core performance.

Note that the multithreaded tests were not performed on the Ryzen laptop because the tests often yielded inconsistent results due to WSL memory limits.

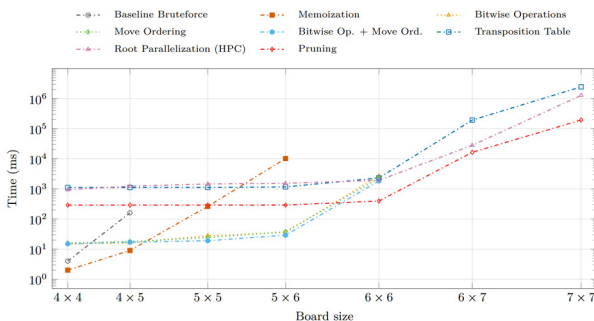


Figure 4: Comparison of solver execution times on a logarithmic scale.

Building on these optimizations, we also integrated a simplified version of the pruning technique used by the Obsequi solver [4].

As the results show (Fig. 4), on an 7×7 board, this solvers' pruned variant ran on a single Ryzen core 6.5× faster than the unpruned multithreaded one on the EPYC CPU.

As expected, introducing multiple optimizations almost always resulted in noticeable improvements.

The only exceptions were the results of testing bitwise operation optimization and heuristic move ordering, since the solver was memory-bound at that point. This anomaly can be observed in Fig. 5.

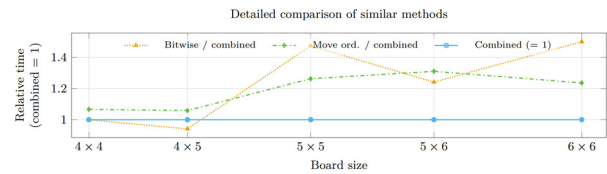


Figure 5: Relative execution times of similarly performing solver variants.

5 Conclusions

Our comparison revealed the effects of different program-level optimizations of an exhaustive Domineering solver.

Memoization avoided repeated evaluation of states, bitboard representation significantly reduced the time spent by the program for evaluating different board states, and a fixed-size transposition table kept the memory usage bounded despite the exponential nature of the problem.

Root parallelization also made better use of the many cores provided by the HPC cluster.

The results demonstrate that data-structure and implementation optimizations can considerably extend the range of board sizes for which a simple exhaustive solver remains practical.

The optimizations alone, however, do not overcome the exponential growth of the number of game states. Solving larger boards therefore still requires strong problem-specific observations and reductions along with an efficient implementation.

6 Acknowledgments

This work originated as a secondary-school graduation project completed under the mentorship of Nataša Makarovič. I would like to thank her for facilitating access to the ARNES HPC cluster and Aleš Volčini for his help in preparing this paper.

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Transforming Python Code into a Single Line

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Abstract: Python uses indentation and line breaks to delimit program blocks, which makes arbitrary programs unsuitable for conversion to a single line by removing whitespace alone. We set out to investigate how much of this structure can be replaced by expressions while preserving program behavior. Our program targets CPython 3.12 and works by transforming source code through an abstract syntax tree. It reconstructs expressions and replaces statements with combinations of lambdas, assignment expressions, comprehensions, generators, and other runtime adjustments. That makes programs with operations that normally require statement blocks able to be one-lined. The program converts a broad range of Python syntax into a single line without using the "eval" or "exec" functions. However, asynchronous iteration, local-variable deletion, several node types, and unresolved edge cases have not been built into the program yet, though they are very close to being implemented. A browser playground allows users to transform code and execute the original and generated versions for comparison. This paper demonstrates the power of Python's expression syntax and CPython's runtime interfaces, while showing that transforming a program into a one-liner can substantially increase complexity and reduce readability. The result is an experimental source transformation tool with applications to studying language semantics and obfuscation.

Keywords: Python; source transformation; abstract syntax tree; one-liner; obfuscation

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1 Introduction

Many programming languages allow most formatting whitespace to be removed without changing a program's meaning. This can be used to minify the source code or make an implementation harder to read. Python presents a different problem: indentation and newlines are used to express statement blocks, so removing them from a program containing functions, loops, or conditional blocks generally destroys its structure.

We set out to make a tool that transforms any Python program into a single line while preserving its original execution steps.

We banned the `eval` and `exec` functions and decided to work with the program's *syntax*.

We selected Python 3.12 and the CPython implementation, because several transformations require access to the interpreter's internals.

The investigation addressed two questions: first, can operations normally written as statements be expressed using syntax that fits inside an expression, and second, can runtime attributes and interfaces of the language's internals reproduce behavior that the built-in syntax cannot express directly.

The solution demonstrates many such transformations, but the goal of converting every Python program remains open due to unfinished constructs.

We also explain the transformation architecture and techniques for preserving evaluation order, scope, and control flow.

2 Transformation Architecture

The implementation and an interactive demonstration are available online [1], [2]. For a better understanding of the following sections, it would be beneficial to briefly study the source code first and have a basic knowledge of the Python language.

2.1 Parsing and Dispatch

The built-in `ast` module exposes Python's abstract syntax tree (AST), including the fields and child nodes associated with each language construct [3]. Parsing the source code into an AST gives us a structured representation that can be traversed recursively. For example, a call to `print` contains a `Call` node, a name identifying the function, and nodes describing its arguments (Listing 1). A `Return` node contains the expression whose value is returned.

```
Module(
  body=[
    Expr(
      value=Call(
        func=Name(id='print', ctx=Load()),
        args=[
          Constant(value='Hello World!')],
        keywords=[])),
    type_ignores=[])
```

Listing 1: an AST tree of the code
`print("Hello World!")`

We implement a handler for each supported node type. The `Handle` decorator registers handlers in a dictionary indexed by node type.

Each handler receives the node, the recursive transformation function, and a shared `Context` object. It returns a string representing the transformed node.

Parent handlers combine these strings into larger expressions until the complete output program is constructed.

Most ordinary expressions can already be expressed as part of a single line and can be re-constructed recursively. These include arithmetic and Boolean operations, comparisons, calls, constants, comprehensions, formatted strings, and conditional expressions. Statements require additional transformations because a lambda body, for example, accepts an expression rather than a sequence of statements.

2.2 Context and Temporary Names

When transforming, each handler receives a context argument containing the transformation state – whether the current transformer is inside a loop, the current scope, information about the current function, and the names used for `return`, `break`, and `continue` state. It also tracks the class namespace, global and non-local declarations, and temporary assignment targets. Handlers save and retrieve relevant context fields when transforming nested nodes.

Generated variable names – used in various workarounds generated by the program – must not collide with names already used by the original source code. Debug mode adds descriptive prefixes while retaining a unique suffix (as seen in Listing 3).

2.3 Evaluation Order and Side Effects

Lists of expressions provide a convenient way to sequence operations – their elements are evaluated in order, and indexing the resulting list can select the value required by the surrounding expression.

Assignment expressions, written with `:=`, bind variables to the current scope. This lets a single expression perform several operations while exposing one final value. It is how most sequences of statements (e.g. in a function or a loop) are implemented in the program.

Sequencing alone is insufficient after an early `return` or a loop-control statement, since executing an expression that would otherwise be

skipped can change the program's behavior. The `Handle` decorator therefore wraps nodes that may have side effects with conditions generated by `prepend`. These conditions prevent inappropriate execution once a control-flow flag is set (in the form of a runtime variable). The `Pure` decorator marks handlers that do not require this protection, such as a handler producing a constant.

3 Transforming Statements into Expressions

Since we can't natively convert the original Python code to be in one line, we must resort to transforming the source code into a single expression.

3.1 Assignment and Unpacking

Assignment targets require different operations. A name can be assigned with `:=`, an attribute with `setattr`, and a subscript through the `__setitem__` method. For chained assignments, an intermediate variable can retain the right-hand value so that it is evaluated once and then assigned to each target. The symbol-table implementation helps identify restrictions that affect assignment expressions [4].

Tuple and list targets are handled through comprehension unpacking. The comprehension binds temporary names, after which assignment expressions copy their values into the intended variables. Reusing the original names as comprehension targets would create scope and rebinding problems. The following two lines in Listing 2 are equivalent:

```
a = b = one, two, three = [1, 2, 3]

([(c := [1, 2, 3]), (a := c), (b := c), [(one := d), (two := e), (three := f)] for (d, e, f) in [c]])
```

Listing 2: Chained assignment with unpacking

The program rewrites an augmented assignment as an assignment whose value is a bi-

nary operation. Annotated assignments additionally update the relevant `__annotations__` dictionary as needed.

3.2 Functions and Early Returns

Function definitions become lambdas after their bodies have been converted to expressions.

Before transforming a function, we save the previous function and scope information, create a new `CurrentFunction` record, and set the scope to the function level. Afterwards, annotations are attached to the generated function, decorators are applied, and the surrounding context is restored.

An early return cannot simply become the final element of the lambda body, as the source may return from a conditional or a loop. We therefore use two temporary variables. A return *flag* records whether a return has occurred, and a mutable *store* retains the return value. A transformed return appends its value to the store and sets the return flag. Later operations are guarded by that flag, and the lambda ultimately retrieves the stored result.

Listing 3 is the generated form of a function that returns 42. The debug prefixes (e.g. `__return_store_`) reveal the separate roles of the flag and value store variables. The store initially contains `None`, providing the default result when no explicit return supplies another value.

```
((forty_two := lambda: [(__return_store_a := [None]), (__return_hit_b := False), (__return_hit_b or [__return_store_a.append(42), __return_hit_b := True]), __return_store_a[-1]][-1]))
```

Listing 3: A function expressed as a lambda

This technique separates the order in which the generated list is evaluated from the control flow represented by its elements.

3.3 Classes and Namespaces

Class definitions use `types.new_class`, which accepts the class name, bases, keyword arguments, and a callback that populates the

class namespace. The context retains the namespace dictionary so that assignments in the class body can update it. The body becomes a lambda, and class decorators are applied after its construction. Methods are generated using the function transformation described above.

This namespace-handling matters, because a class body and an ordinary function body do not bind names in the same way: binding a name in a class body also makes it a static property of the class.

Recording the active scope allows assignment handlers to change the class namespace as well, along with binding the names to the surrounding scope.

3.4 Conditions and Loops

Conditional statements become conditional expressions. If there is no else branch, short-circuit evaluation can express the operation in the form `(condition) and [body]`. The body is evaluated only when the condition is true.

A for loop becomes a comprehension [9]. However, a comprehension's iteration variable is local to that comprehension, whereas the corresponding name in a statement loop remains available in the surrounding scope. The transformer therefore uses a temporary iteration name and explicitly assigns its value to the intended variable on each iteration. Listing 4 preserves the variable `i` while printing the numbers from 1 to 10:

```
(([[[(i := a), (print((i + 1)))] for a in range(10)]])
```

Listing 4: A for loop represented by a comprehension

Loop handlers also create state for break and continue when needed. The continue flag is reset at the beginning of each iteration, and runtime guards control whether the remaining body is evaluated (like the return functionality in functions). Attribute and subscript targets need separate treatment because they assign to existing objects.

For while, the implementation combines a generator with a consuming comprehension. The generator uses an unbounded iterator and yields condition values while arranging the body evaluation. A second iterator repeatedly advances the generator until the sentinel value `False` is returned. This provides a way to express repeated conditional execution through expressions.

3.5 Exceptions and Context Managers

Python has no general expression equivalent for the try statement.

We use `contextlib.ContextDecorator` to obtain exception information through a generated object's `__exit__` method. A decorated callable advances a generator containing the body, and the exit method selects the corresponding exception handler when an error occurs.

Generators are useful here, because they delay execution without requiring the protected statements themselves to become the body of a newly introduced lambda. Assignment expressions inside the generated comprehensions can refer to their containing scope.

The implementation uses one-shot generators for the protected body and other deferred blocks, and a mutable collection to pass an exception into the appropriate handler.

The else and finally blocks are advanced along the relevant normal and exception-generating paths.

The code in Listings 5 and 6 demonstrate the conversion between the source code and its one-liner equivalent.

```
try:
    1 / 0
except ZeroDivisionError as e:
    print(f"Caught error: {e}")
```

Listing 5: A sample program catching a zero-division error

```
((a := [], b := [(1 / 0)] for _ in [0]), (i :=
[print(f"Caught error: {e}") for e in a]),
type("h", (__import__("contextlib").ContextDecora-
tor,), {"__enter__": lambda f: f, "__exit__": lam-
bda f, d, c, g: [c and (a.append(c) or ((*i, if
isinstance(c, ZeroDivisionError) else
None))]})))(lambda: (*b,))())
```

Listing 6: The one-line equivalent of the code on Listing 5

Context managers reuse this concept. The transformation evaluates the manager, calls `__enter__`, binds its result, and arranges for `__exit__` to receive the exception information, following the behavior described for the `with` statement [5]. Asynchronous context managers require the corresponding `__aenter__` and `__aexit__` operations and await handling.

Raising an exception can be expressed through a generator's `throw` method. The same mechanism implements an assertion by raising `AssertionError` only if its condition is false. Raising chained exceptions also sets the raised exception's cause. Listing 7 illustrates this mechanism.

```
(a or (_ for _ in ()).throw(AssertionError('')))
```

Listing 7: An assertion represented by an expression

3.6 Pattern Matching and Imports

For a `match` statement, the subject is evaluated into a temporary variable. Each case becomes a sequence of tests for its pattern and optional guard, followed by the transformed body when the tests succeed. Sequence patterns require checks on the subject's type and length, followed by assignments for captured names. The language reference describes the conditions associated with the different pattern forms [6].

Imports use `__import__`. An ordinary import binds the module to its name or alias, and a `from-import` retrieves the required attributes from the imported module. A wildcard import uses `__all__` when available or selects public names from the module dictionary.

4 CPython Runtime Operations

One could say that Python is a bit too familiar with its inner workings. We exploit this to implement statements that cannot be expressed using normal Python syntax.

4.1 Asynchronous Functions

A lambda cannot directly express an `async def` declaration. The solution is to generate a function using `yield from` as the `await` keyword and then replace its code object to change the execution flags.

The CPython compiler and symbol-table sources were used to examine the relationship between these constructs and their restrictions [4], [7].

In the transformation shown in Listing 8, `main` is the generated function and `a` is a temporary variable. The bit operation clears `CO_GENERATOR` (32) and sets `CO_COROUTINE` (128). The replacement is applied after creating the function and before applying its decorators.

```
setattr(main, '__code__', (a :=
main.__code__).replace(co_flags=a.co_flags & ~32 |
128))
```

Listing 8: Changing a generated function's code flags

Asynchronous iteration also requires explicit iterator protocol operations, including `__aiter__` and `__anext__`, as described by the language reference [8]. The program's asynchronous iteration coverage is not yet ready for publication.

4.2 Global and Nonlocal State

The `global` and `nonlocal` statements affect subsequent name resolution and assignment. Their handlers record declared names in the context. Assigning to a global name updates the global namespace dictionary. For a non-local assignment, the prototype accesses the enclosing closure cell through the generated

function's `__closure__` attribute and determines its index using `__code__.co_freevars`.

The cell is then updated using CPython's `PyCell_Set` interface through `ctypes`. This reproduces the required mutation without a `nonlocal` statement in the generated lambda.

Deleting a local name is more difficult because changing a frame's locals dictionary does not necessarily update the function's active local variables. We investigated removing the entry and calling `PyFrame_LocalsToFast` to synchronize it.

This technique was not sufficiently tested and was therefore excluded from the current version of the program. Attribute and item deletion have more direct expression-based operations, using the `delattr` and `__delitem__` functions respectively.

5 Results and Limitations

The solution demonstrates that a substantial set of Python constructs can be represented in one line by combining expression syntax with runtime operations. Assignments, functions, classes, conditions, loops, exception handling, imports, and scope-sensitive updates can all be represented using expressions.

The browser playground [2] runs the transformer locally through Pyodide, which provides a WebAssembly-based Python environment. Users can enter a program, inspect its transformed source, and execute the original and generated versions to compare behavior.

We tested one-lining an already one-lined program and determined that the process yields the same output (disregarding spaces or additional parentheses).

5.1 Remaining Work

The solution defers asynchronous iterators and loops, local-variable deletion, and `yield`

inside loops for later. It also omits several AST node types, including `TypeAlias`, `TypeVar`, `ParamSpec`, `TypeVarTuple`, and `TryStar`.

Generated state and additional expression layers also increase the complexity of the output. A single line is not necessarily smaller source code, and the generated comprehensions, lists, and runtime calls can introduce overhead.

Future work should complete the missing handlers and test combinations of nesting, scope changes, and exceptional control flow. Care is particularly necessary where simplified assignment rules, asynchronous execution, or access to interpreter internals may differ from the source program's behavior.

6 Conclusions

We developed an AST-based prototype that converts source code based on a broad range of Python 3.12 syntax into one physical line.

The core techniques are having explicit control-flow state, scope-aware assignment, and special workarounds for complex statements. Generators and context managers provide delayed and exceptional execution, and CPython interfaces support operations that are difficult to reproduce with expression syntax alone.

The work demonstrates the feasibility of substantial source transformation despite Python's dependence on indentation. Complete language coverage remains a development goal. The implementation and playground provide a basis for examining these transformations and testing their semantic limits.

Even using the solution to parse itself is successful, however, Python refuses to run the program due to "too many nested parentheses". We left this problem for later, but we're looking into a solution using a system for isolating statements to avoid this limit.

7 Acknowledgments

The author thanks the mentors Matic Podpadeč and Aleš Volčini, for their time, advice, and assistance throughout the research.

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9 Additional remarks

For this article, the listings are packed to conserve space. However, they could be expanded and therefore be more readable.

For example, in Listing 6, we see the code:

```
((a := [], b := ([1 / 0]) for _ in [0]), (i := ([print(f"Caught error: {e}") for e in a)), type("h", (__import__("contextlib").ContextDecorator,), {"__enter__": lambda f: f, "__exit__": lambda f, d, c, g: [c and (a.append(c) or ((*i,) if isinstance(c, ZeroDivisionError) else None))]})(lambda: (*b,))()))
```

This code is supposed to be in one line. However, if we format it using Python's official style guide (PEP 8), we can see the former expression in a now readable form:

```
(
    (
        a := [],
        b := ([1 / 0] for _ in [0]),
        (i := ([print(f"Caught error: {e}") for e in a)),
        type(
            "h",
            (__import__("contextlib").ContextDecorator,),
            {
                "__enter__": lambda f: f,
                "__exit__": lambda f, d, c, g: [
                    c
                    and (
                        a.append(c)
                        or ((*i,) if isinstance(c,
ZeroDivisionError) else None)
                    )
                ],
            },
        )()
    )(lambda: (*b,))(),
)
```

This formatting of the expression shows its structure in a concise way. It still counts as one line, since the whitespace can be omitted while the meaning of the code in Python stays the same.

Research and construction of a hard beta and gamma sensitive Geiger counter

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Abstract: This project combines physics, software, and electrical engineering in the design and construction of a low-cost Geiger counter based on the Soviet SBM-20 Geiger-Müller tube and an ESP8266 microcontroller. The detector uses a high-voltage supply, an external probe, an analogue ammeter, and adaptive digital smoothing to provide stable but responsive count-rate measurements. After construction, the instrument was tested at the Milan Čopič Nuclear Training Centre using an Eu-152 source. Background-corrected count rates were measured at different source-detector distances to investigate the inverse-square dependence of gamma-radiation intensity. The measured count rate decreased clearly with increasing distance, although more slowly than the ideal inverse-squared relationship. The deviation is most likely caused by the finite geometry of the detector and scattering of gamma radiation in surrounding materials, while dead-time losses were found to be negligible. The results demonstrate that the constructed device is suitable for qualitative and quantitative radiation measurements.

Keywords: ESP8266; SBM-20; gamma radiation detection; signal processing

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1 Introduction

Geiger counters are among the simplest and most recognized radiation detection devices, but commercially available instruments can be relatively expensive, especially for hobbyists or radiation enthusiasts.

The motivation for this project came from my interest in radiation and the wish to build a functional Geiger counter from readily accessible components.

The aim of the project was to design and construct a functional device and evaluate its performance by experimentally investigating the dependence of the gamma radiation count rate on the distance from the source.

2 Principles of operation

To understand the building process, let's look at some basics first.

2.1 Geiger-Müller detection principle

A Geiger-Müller (GM) tube is a gas-filled detector used for detecting ionizing radiation [3]. It consists of a cylindrical cathode and a thin anode wire running through the centre. The tube contains a noble gas mixture and operates under an applied high voltage.

When a high-energy particle enters the tube, it ionizes the gas, producing free electrons and positive ions. The electrons are accelerated by the electric field, which causes further ionization, creating an avalanche effect. This results in a short electrical pulse that can be

detected and counted by subsequent electronics.

Due to the nature of its design, a GM tube cannot determine the energy of the particle; and therefore, a Geiger counter like mine cannot be a dosimeter.

2.2 SBM-20 Geiger-Müller tube

The SBM-20 is a Soviet GM tube intended for the detection of high-energy beta (beta particles to penetrate the wall of the detector) and gamma radiation [1].

Unlike thin windowed GM tubes, which can also detect alpha radiation, it uses a cylindrical brass body, 0.05 mm thick¹. The tube is filled with a mixture of Ne, Ar, and Br₂.

Neon acts as the primary ionization gas, a small amount of argon helps with lowering the required voltage, and bromine quenches the avalanche after it happens, absorbing energy and preventing ghost pulses.

I chose the tube due to its widespread availability and inexpensiveness.

2.3 Count rate and statistical fluctuations

Each discharge of the GM tube produces a pulse that is counted by electronics. The detector response can therefore be expressed as a count rate, usually in counts per second (CPS) or per minute (CPM).

Because radioactive decay is a random process, counts fluctuate even under constant conditions.

These fluctuations are approximately described by Poisson statistics, meaning that the relative error is larger at low count rates and decreases as the number of detected events increases ($\Delta n = \sqrt{n}$) [3].

For this reason, the measured count rates are usually smoothed before being displayed, creating a trade-off between reading stability and response time.

3 Design

The finished device consists of an external detector probe, using the aforementioned SBM-20 tube, a high-voltage supply, an analogue display, an active buzzer and the ESP8266 microcontroller (Wemos D1 mini) on a custom designed PCB.

It also contains the detection circuit, which converts each discharge into a pulse, suitable for the microcontroller.

The ESP8266 counts, processes and displays these pulses on the analogue meter, while an LED and buzzer provide an indication of individually detected events.

3.1 Initial high-voltage circuit

The initial design used a discrete switching high-voltage converter shown in Fig. 1 to generate the operating voltage required by the SBM-20 tube, which is around 400 V.

To obtain a hopefully stable high DC voltage, the circuit employs an inductor L1, switched by the MJE13001C1 transistor (Q1), followed by a diode D1 and a 0.01 μ F capacitor C1.

During testing, however, the circuit proved very unreliable and often did not work at all; a possible cause is that the Q1 transistor sustained damage from induced spikes of higher voltage when interrupting the current through the inductor.

¹ A weakness I quickly discovered when purchasing the tube from eBay

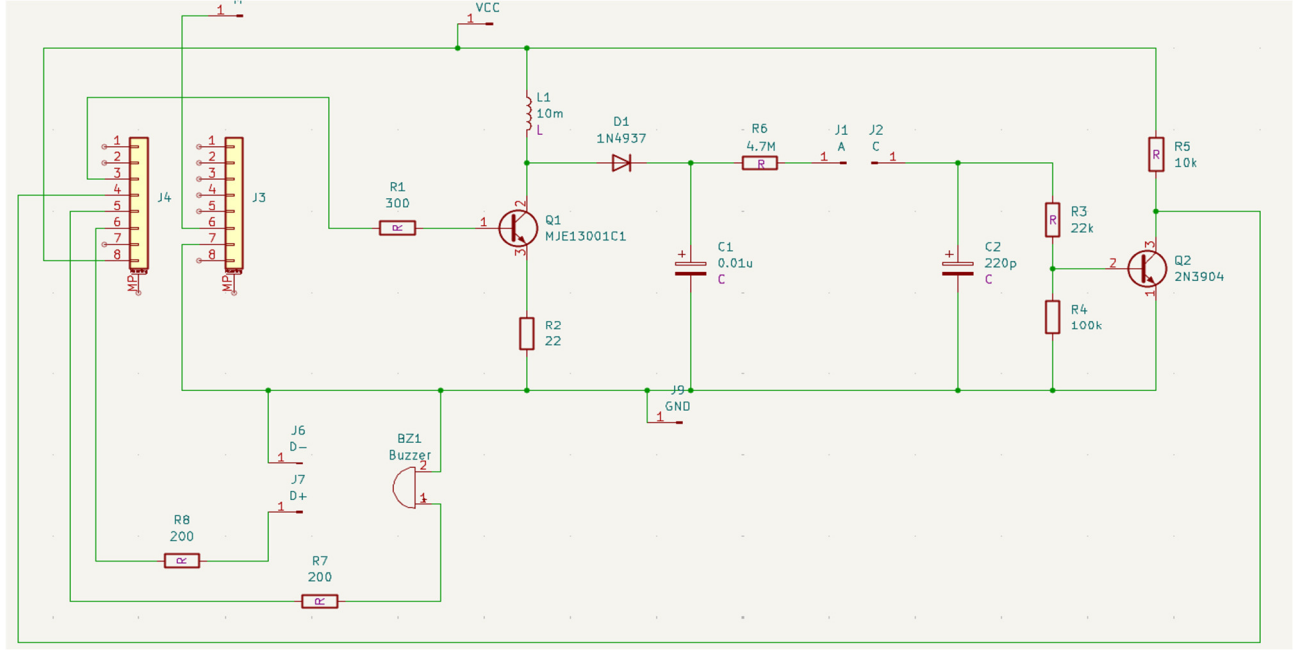


Figure 1: Initial circuit design, adapted from schematics from Hackaday [2].

3.2 Detection circuit

The detection circuit on the right side of the schematic in Fig. 1 consists of a 2N3904 transistor (Q2), whose base is driven by the capacitor C2, which discharges through the voltage divider (R3 and R4).

The pulse from the GM tube deposits a charge in C2, which causes the transistor Q2 to conduct briefly. As a result, the collector voltage is pulled close to ground, producing an active low pulse that is detected by the ESP8266.

3.3 Digital processing

The ESP8266 microcontroller counts, processes (smooths), and displays CPM or CPS.

To minimize the probability of missing pulses, counting is done using an interrupt routine attached to pin D5 (GPIO14). The pulse rate is evaluated every $\Delta t = 250$ ms, with four consecutive measurements combined into a rolling interval of approximately one second.

Adaptive exponential smoothing of the measured CPS (x_k) is achieved by running two exponential smoothing filters using the raw

measured rate (r_k) with different time scales (Eq. (0)):

$$x_k = x_{k-1} + \alpha(r_k - x_{k-1}), \quad (0)$$

where $\alpha = 1 - e^{-\Delta t/\tau}$.

The fast filter operates with a time constant (τ) of 1 s and is used to detect sudden increases or decreases in radiation intensity. The slow filter provides the actual value used for the meter and adapts its time constant to the measured count rate.

At low count rates, where statistical fluctuations are large, stronger smoothing is applied, with $\tau = 30$ s.

As the count rate increases, the time constant is reduced to a minimum $\tau = 0.5$ s. If the fast filter detects a significant change, the slow filter is temporarily accelerated. This provides stable readings at background radiation levels while still allowing a rapid response when a stronger source is introduced/removed.

The device reports radiation event counts in multiple ways: an active buzzer, an LED diode, an analogue ammeter (fig. 2) and a website that the ESP8266 hosts on its own network, enabling easier debugging.

The buzzer and diode work on a simple logic where each pulse is represented by one “ping” or one flash respectively. At the same time, the ESP8266 generates signals using pulse width modulation (PWM) which drives the display, showing CPM on a scale 0-50, while a toggleable x10 switch enables the scale to show 0-500 CPM.

4 Construction

The PCB mentioned in chapter 3 was designed in KiCad and fabricated by JLCPCB.

Because of the problems with the HV supply, I decided to replace that part of the circuit with a high-voltage DC-DC step-up converter, powered directly by the 3.3 V bus.

That resolved the issues with the supply, but increased power consumption, which was an acceptable compromise for improved reliability.

I designed a housing for the electronics and the tube in Fusion 360, basing the design loosely on the IMD-5 soviet Geiger counter. It was printed using PLA plastic in an FDM printer. The holder for the probe was designed and printed in a similar way.



Figure 2: the device viewed from the top.

A bigger challenge came when designing the housing for the GM tube, because I wanted something that wouldn't compromise the sensitivity, while providing sufficient mechanical protection. For the anode and cathode to

be well isolated from each other, I used BNC connectors to connect the probe to the body.

The body of the probe consists of a 0.5-mm-thick aluminium cylinder, extracted from an alcohol marker (Fig 3). Aluminium was chosen, because the attenuation by PLA of the same thickness appeared to be higher.

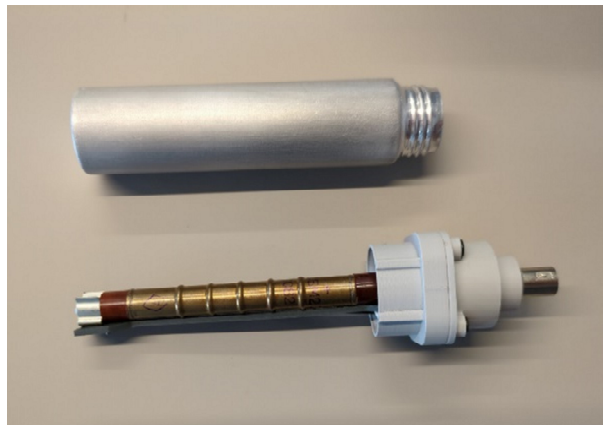


Figure 3: an overview of the probe showing both the SBM-20 tube and the aluminium housing.

5 Experimental verification of the inverse-square law

After the device was built, I only had access to an old compass, which had dials painted with Ra-226. That showed that the device responded to sources, allowing the smoothing to be adjusted.

But as that was my only source (excluding background radiation), I decided to contact the Milan Čopić Nuclear Training Centre (ICJT), asking for help with testing my device. Their expert recommended we focus the experiment on measuring gamma radiation.

5.1 Experimental setup

At the ICJT, we decided it would be best to use the Geiger counter to test the inverse-square law on an Eu-152 source (fig. 4), since it was new and its activity was 10 times that of the alternative candidate, Sr-90.

To achieve consistent results, a β -shield was constructed using concrete and plastic (fig. 5).

The probe was immobilized on a movable vice, and two lead plates were added on the bottom to prevent backscatter (of gamma rays) from the table below.

The experiment consisted of first measuring three reference background count rates, each over a period of one minute. An average was then calculated, which was approximately 44.8 CPM.

This number was later subsequently subtracted from the measurements to get the desired Eu-152 value.

At the same time, this number also represented the upper limit of useful information. That is because count rates that were lower than two times the average background CPM had large margins of error.

On the other hand, a lower limit was set to around three times the maximum diameter of the source between it and the GM tube. This was also completely practical as the shield itself did not allow the vice to go any lower than 4 cm away from the source.



Figure 4: The Europium source, with an activity of 1 μ Ci, measured in august of 2024.

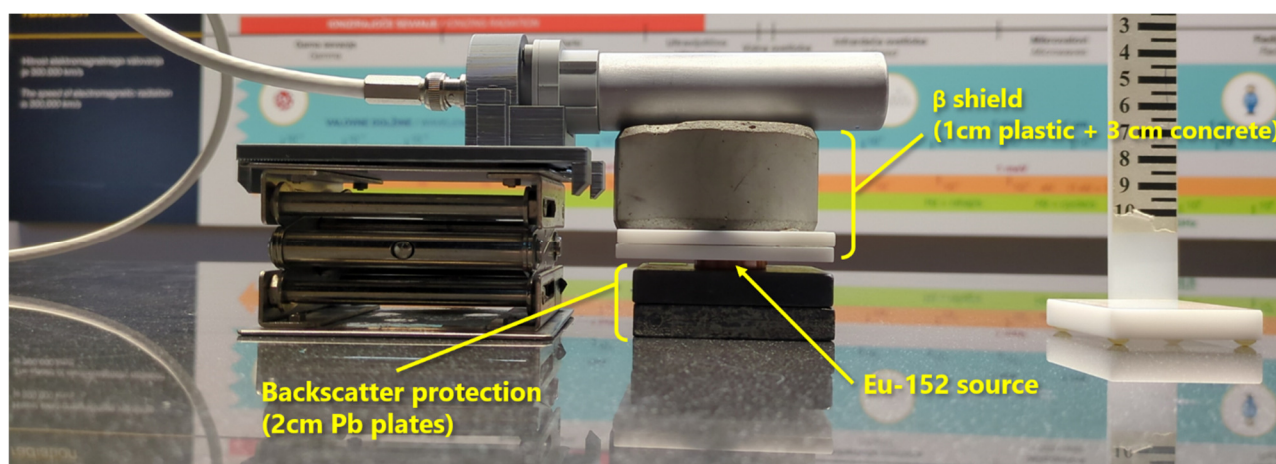


Figure 5: Side profile showing the experiment.

5.2 Measurement procedure

First, we tested the Sr-90 source at 6 cm, with and without the β -shield. It turned out that after applying the shield, count rates in one minute did not differ from the background, meaning that the Sr-90's beta emission attenuated by the shield yielding counts indistinguishable from background.

That is why it was decided to switch to Eu-152. The measurements were started again at 6 cm, and all subsequent measurements were done with the β -shield. Every measurement took 1 minute, after which the background CPM rate was subtracted, and the GM tube was moved 1 cm further away.

This was done 10 times, until the readings stopped being reliable at 15 cm (50 CPM vs 44.8 reference). At that point, we decided to

go in the other direction, and the distance was lowered from 6 to 4 cm. All results were later graphed.

6 Results and discussion

The measured background-corrected count rate decreased as the distance between the Eu-152 source and the detector was increased (Fig. 6).

The count rate decreased from approximately 208 CPM at 4 cm to approximately 35 CPM at 15 cm. This clearly demonstrates the expected decrease in gamma-radiation intensity with distance.

For an ideal point source and point detector, the radiation intensity is expected to follow the inverse square law ($R(r) = \frac{A}{r^2}$), where $R(r)$ is the background-corrected count rate, r is the distance between the source and the GM tube and A is the proportionality constant.

Although the measured data follows the decreasing trend, the count rate is falling more slowly than predicted by an ideal $\frac{1}{r^2}$ dependence.

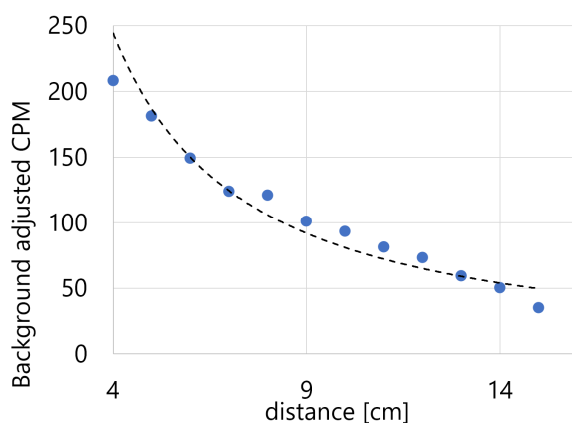


Figure 6: Dependence of the background-adjusted CPM as a function of the distance to the source.

Several effects may contribute to this difference. Firstly, the assumptions of a point source and a point detector are not fully valid

at short distances (Pythagorean triangle tells us that the difference between the hypotenuse and the longer cathetus is bigger, the shorter they are), and this applies to the SBM-20 as it is a cylinder.

This means that the ends of the tube sit at noticeably different lengths from the source, influencing the observed dependence.

A second possible explanation is that of gamma radiation scattering in the beta shield and surrounding materials. Gamma photons can undergo Compton scattering and enter the detector from directions other than the direct source-detector path.

Since a GM tube provides no information about energy of the particles, these scattered photons cannot be distinguished from the ones arriving directly from the source. This contribution could be the cause of the slower count rate decrease.

Another possible reason was dead-time losses, as multiple counts would be interpreted as only one. However, taking the highest calculated raw rate (253 CPM), and dividing by 60, that only comes out at around 4.2 CPS.

Considering the dead-time of the SBM-20 tube, which is around 190 μ s plus the dead-time of the detection circuit (around 50 μ s), the expected fraction is below approximately 0.1 % and is therefore too small to explain the observed deviation.

Despite these limitations, this experiment demonstrated both the sensitivity and fast response time of the constructed detector and showed a clear distance dependence consistent with the expected behaviour of gamma radiation.

A possible continuation of the experiment would be to repeat the measurements using the same setup but using a scintillation detector (Radiacode 103 or similar), as those can filter out lower-energy scattered photons from direct gamma rays, helping to determine the

contribution of scattering to the observed result.

7 Conclusions

The project successfully demonstrated that a functional Geiger counter can be constructed from generally accessible components using an SBM-20 GM tube and an ESP8266 micro-controller.

The final device was able to reliably detect background radiation and radioactive sources, while the smoothing of count rates provided a good balance between stable readings and responsiveness.

Measurements performed with the Eu-152 source showed a clear decrease in counts, as the distance increased, consistent with the inverse-square behaviour.

Although the decrease was slightly slower than that of the ideal dependence, this could be further explored by doing follow-up experiments.

8 Acknowledgements

I would like to thank the Milan Čopič Nuclear Training Centre (ICJT), and especially Urban Pompe, for providing access to radioactive sources, and helping me immensely with the experiment and understanding of radiation and nuclear instrumentation.

At the same time, I had a lot of help regarding the smoothing, as that was a complex task requiring knowledge of statistics and more mathematics than I have. For that, I thank my father, a particle physicist, who helped me understand the basics of statistics and helped me design the principles of smoothing.

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Research and Development of a Smart Two-Stage Model Rocket

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Abstract: We present the various elements of mechanical, electrical and software engineering needed for a technically advanced two-stage model rocket. We describe the design, implementation, simulation and testing of individual components, covering tasks such as ignition, propulsion, stage separation, flight control, communication, telemetry and recovery. In addition, we ponder the challenges of writing software in mission-critical environments, where every mistake is a potential critical failure. Finally, we evaluate the recorded experimental data and discuss the potential uses of the project, specifically within the Noordung Labs student rocketry project.

Keywords: model rocketry; two-stage model rocket; 3D-printing; embedded software; microelectronics

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1 Introduction

Amateur model rocketry is typically not a field of research done by high schoolers, as it requires intimate knowledge of various different fields, as well as years of practical experience. Furthermore, most amateur rocketry projects rely purely on mechanical methods of flight control, rarely incorporating electronics at all.

We wanted to see if we were, with the help of our much more knowledgeable mentors, capable of producing a technically advanced, two-stage model rocket that incorporated home-brewed electronics not only to capture experimental data, but also to perform flight-control tasks.

2 Materials and Methods

For the body of the rocket, we used laminated cardboard tubing. Despite cardboard being a

weak material on its own, the laminated structure and proper processing make it a very lightweight and rigid component.

We also heavily relied on FDM 3D-printing. The majority of the complex parts from the engine mounts to the transition and nose cone were 3D-printed. This opened up the possibilities of manufacturing more complex parts than we would otherwise be able to produce. We used filaments such as normal PLA (sourced from local providers), and we also experimented with a lightweight version using LW-PLA. Due to the nature of 3D-printing, there is minimal need for processing the parts.

For the rocket's fins, we used balsa wood due to its low density.

The finishing touch involved a lot of sanding and gluing.

A lot of the mechanical design was based on simulations we did in the open-source software OpenRocket [1], which is used for simulating model rockets. We built and optimized the whole model of the rocket in the simulation.

Before we did any of the manufacturing, the rocket was entirely 3D-modelled in a CAD (computer-aided design) program, Onshape [2]. We made every part from the nose cone to the engine mounts to make sure everything would fit together. This also allowed us to 3D-print parts right away.

3 Initial Design

In the initial design phase, we decided to build a rocket that had two stages because of the additional unique learning opportunities and design challenges this would entail. We also discussed the benefits of the higher apogee altitude and longer airtime for more and better sensor data. We also knew we would only use off-the-shelf model rocket motors, primarily due to safety and reliability concerns.

3.1 Body Tubes

As mentioned before, the body tubes were made from laminated cardboard tubing. The lower stage has one that is 80 mm in diameter and 300 mm long, and the upper stage has one that is 50.8 mm in diameter and 400 mm long.

Before the flight, the tubes had to be processed. This included sanding the outer layer off and applying several coats of varnish. After each coat, the body tube had to be sanded down until it was smooth.

Another important step was filling the gaps left from the laminating of the cardboard. This was done by applying a mixture of varnish and talc (often found in baby powder). After sanding the surface until it was smooth and the gaps were filled, the tube was ready for painting.

3.2 Fins

The rocket achieves stability by manipulating the position of the center of gravity, C_g , and the center of pressure, C_p [3]. The latter is done with aerodynamic components – fins. When building a model rocket, the most common fin configurations are three or four fins per stage [4]. Four-fin configurations are typically used in guidance applications, because they provide easier manipulation of the air-flow across the rocket. However, if the rocket is unguided, it is better to only use three fins to achieve less aerodynamic drag.

The most common shapes for rocket fins are trapezoidal and elliptical [4]. For our rocket, we used a modified trapezoidal shape (see Fig. 1). The lower stage uses quite large fins with an area of approximately 104 cm². The upper stage also uses quite large fins for its size – approximately 70 cm².

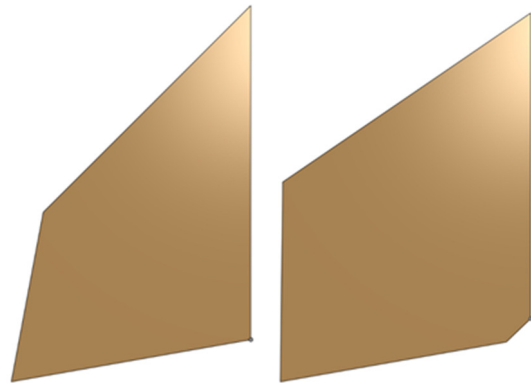


Figure 1: Upper fins (left) and lower fins (right), not to scale

The fins had to be properly processed prior to the flight. The processing is pretty much the same as for the body tubes. It included sanding, applying varnish and talc. One different but very important step specific to the fins is to sand the upper and lower edges of the fins into an airfoil cross-section. This significantly decreases the drag experienced by the whole rocket.

3.3 Motors and Engine Mounts

The rocket uses solid-fuel model rocket motors, specifically 6 D9-5 motors in the lower

stage and 4 D9-P motors in the upper stage. They are off-the-shelf rocket motors and the most powerful ones that we could find. The “D” classification means that they produce 20 Ns of impulse; “9” means they produce 9 N of average force throughout the whole burn.

The “5” at the end is the time, in seconds, between the burnout of the motors and the explosion of the ejection charge. The P just means that the motors are plugged and they do not have an ejection charge [5][6].

The engine mounts are designed to hold the motors securely and to provide sufficient structural strength to withstand the forces from the ejection charges. They also provide a secure place to attach the shock cord for the recovery device.

3.4 Transition

The transition serves as an adapter, connecting the two stages of the rocket together.

In the first iteration, it also served as a launch lug and a housing for the electrical components. It also serves as a mount for the shock cord, parachute and second-stage ignition system.

It is a 3D-printed component, making it very easy to manufacture, although the shape is quite complex.

3.5 Nose Cone

Another very important aerodynamic component is the nose cone. It serves as the housing for the electronics in the upper stage. It also plays a critical role in the rocket's aerodynamic performance, heavily impacting its coefficient of drag, C_x .

Some of the most common nose cone shapes include conical, ogive and ellipsoid shapes. They differ in their coefficients of drag [7]. We used a tangent ogive nose cone.

3.6 Recovery Device

The recovery device is used to make sure that the stages of the rocket come back to the ground safely. To achieve this, the most common tool is a parachute; however, one could also use a streamer. For both stages of our rocket, we used parachutes made from rip-stop nylon, measuring 100 cm in diameter.

The parachutes are connected to the transition and the nose cone in the upper stage, and they are all connected to the engine mounts with a roller shutter tape in the role of the shock cord. The recovery devices are deployed with the previously mentioned ejection charges of the motors and the extra deployment charge we made in the upper stage.

3.7 Launch Device

At the start of the rocket launch, the rocket is not producing enough thrust to have a stable flight. To solve this problem, a launching device is used [8].

For our rocket we used a 150-cm-long and 5-mm-diameter rod as a launch rod. To connect it to the rocket we had a hole going through the lower stage engine mount and the transition.

On the upper stage we had a 3D-printed launch lug in the shape of a droplet. This, however, proved to be suboptimal, as sometimes the transition would rotate and cause severe friction against the launch rod.

To start the motors, one can use the provided electrical igniters, but they are not very reliable. With only one motor this is not such a problem, as it can be ignited again.

However, using a cluster of motors poses a much greater risk, due to the sideways torque produced by having only some of the motors ignited.

That can have serious consequences such as making the rocket flight unstable and causing it to spin out of control, damaging itself, and presenting a safety risk.

To solve this problem, we used a small aluminum can, inside which we ignite a small amount of black powder. We soldered some springs onto the top face, which guide the flames into each motor.



Figure 2: The lower ignition device

We used a similar system to ignite the motors of the second stage. Instead of using aluminum, we 3D-printed the compartment, gluing a piece of sheet metal with the soldered springs onto the plastic.

3.8 Electrical Design

The rocket's electrical systems have three main purposes: most importantly, they are responsible for flight control, meaning the first stage must deploy the second, and the second must activate its parachute deployment charge; they should ease recovery by transmitting the rocket's location; and they should log sensor data and controller state for research and debugging purposes.

Starting with flight control, we trigger the igniters by charging a large, 2.5 F supercapacitor to 5 V through a 20-ohm resistor (limiting the current to 250 mA) over a relay, which we then power through a common bipolar junction transistor (S8050) to switch the positive terminal of the capacitor to the igniter (Fig. 3).

We opted for such a large capacitor, as we were still unsure how much energy was required to fire our igniters, since this can vary

significantly between models and manufacturers [9]. Still, we found the resulting 31.25 J to be more than enough.

We were able to construct this circuit quite easily, as the large capacitor is the only uncommon component. The main caveat we foresaw at this stage was the need to properly orient the relay, as otherwise the large upward launch force could move the relay into a premature open state, triggering it instantly.

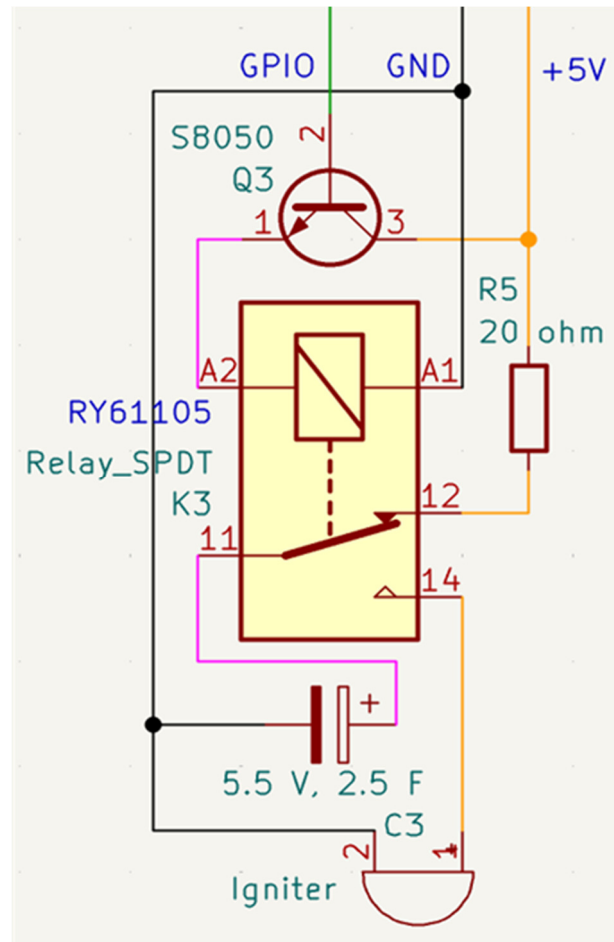


Figure 3: Initial ignition circuit

For the sensors, we opted to measure air pressure (to derive altitude), motion (acceleration and angular velocity), and absolute position.

We achieved this with a BME280, MPU6050 IMU (lower stage), ICM20948 IMU (upper stage) and GY-NEO6MV2 GPS module. We decided to save the measurements to a microSD card. Communications (for aided recovery and telemetry) were done using APC220 RF transceivers.

As our simulation showed a peak acceleration of 212 m/s^2 , well above our IMU's full-scale maximum of 16 g [10] [11], we decided to mount it at an angle of 45° , splitting the vertical axis along two sensor axes, expanding the maximum to 22.6 g .

We decided to use the Raspberry Pi Pico 2 as our main microcontroller, as it includes hardware support for all major embedded communication protocols, has a very well-written and well-documented SDK, 26 GPIO pins, and two 150-MHz cores [12]. It also allows us to use both low-current 3.3 V and high-current 5 V electronics, as its internal 3.3 V voltage regulator supports up to 300 mA of current drain [13], and its GPIO pins are fully 5-V-tolerant [14]. This allows us to wire the low-power BME280 and IMU to 3.3 V, while allowing the power-hungry APC220, GPS, and ignition circuits to draw directly from the 5 V batteries (Fig. 4).

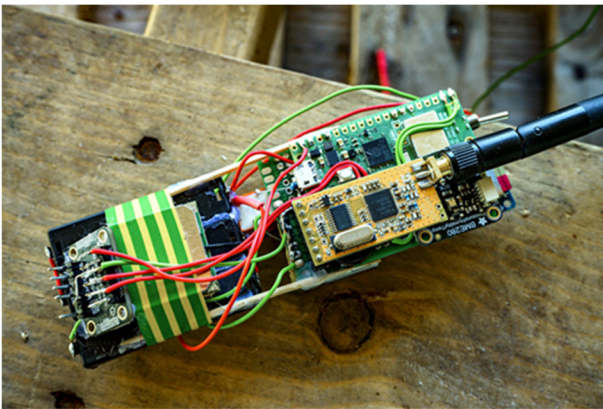


Figure 4: Assembled upper stage controller

For the batteries themselves, we decided to use three off-the-shelf AAA batteries, usually reaching about 4.8 V when wired in series, instead of perhaps one rechargeable lithium pouch cell. We recognize the latter choice may have allowed us to save a small amount of weight, but we reasoned that the benefits of always using new batteries (without any wear) and the ease of acquiring replacements (a trip to the nearest gas station) greatly outweighed this.

3.9 Software Design

The main module software was written in C++. We opted not to use advanced standard library structures such as smart pointers for performance reasons.

We completely avoided heap allocations for the same reason. Most structures (including buffers for receiving and sending data) are statically allocated to minimize the risks of potential buffer overflows or memory-related bugs.

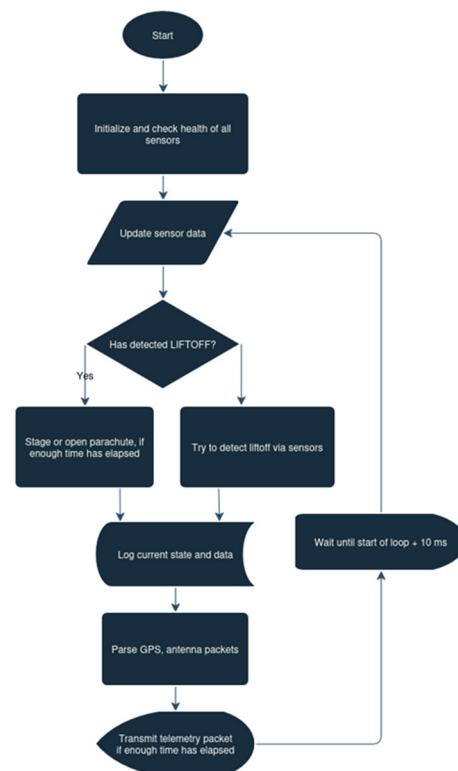


Figure 5: Simplified main control loop

We decided to write as much of the code as possible ourselves, partly as an educational experience and partly, again, for performance reasons. The only dependencies we used were the official RPi Pico SDK [15] and pico-fatfs-sd [16], an open-source library for using the FAT filesystem with an SD card over SPI.

Our main control loop (Fig. 5) is as follows: we read the latest sensor data, check if we need to perform any flight-control actions, log the sensor data in our own minimal-overhead bi-

nary format, process antenna and GPS packets, and finally send a telemetry packet if enough time has passed.

Flight-control actions boil down to detecting a potential launch. Once we have detected it, we simply record the liftoff time and prime the timers for other actions (deployment of the second stage or parachute) with delays estimated by our simulation [17].

4 First Flight

We arranged for a launch window on the 4th of July, between 11:00 and 13:00, at the Poček training ground under the jurisdiction of the Slovenian Armed Forces. We arrived on site early and began preparing the rocket.

During the final checks of the electronics, we were surprised to discover the ignition system's relay did not fully switch open, leaving the output at 0 V.



Figure 6: The rocket shortly after ignition

We theorized this was caused by a slightly low battery voltage (e.g., 4.7 V vs. 5.0 V), as well as high temperatures ($> 30^{\circ}\text{C}$) increasing the relay coil's resistivity. We temporarily remedied the problem by switching in new batteries and cooling down the modules.

We successfully launched the rocket (Fig. 6). At the time, we believed that we had seen the second stage deploy far too late, and its engine compartment explode, as we saw a clear trail of one of the motors spiraling off into a random direction.

The bottom stage successfully opened its parachute and glided to the ground, whereas the top stage was less fortunate, falling to the ground at its terminal velocity.

We were able to recover both, though the top body and nose cone were fractured into several pieces (Fig. 7). The upper electronics compartment batteries had also broken apart, causing the module to lose power.



Figure 7: Both stages after the first launch

4.1 Results of the First Flight

We were only able to recover the lower controller's flight log, as we found the file on upper stage's SD card empty.

Still, we were able to draw useful conclusions from the first stage's sensor data and flight log. Most importantly, the reported ignition of

the second stage (from the first) did not correlate with any such event in the recorded video.

We believe this was caused by the same issue that we tried to remedy on the ground, with the module heating up and batteries discharging slightly during the final stages of launch preparation.

The actual ignition of the upper motors and subsequent explosion are consistent in timing with the lower parachute ejection charge, which we believe may have mechanically triggered the relay to open.

As for the actual motor explosion, we can only speculate, but possible causes include manufacturing faults and degradation due to storage conditions, particularly moisture [18].

To interpret the IMU data, we built a system to recreate the lower stage's flight path by integrating the measured acceleration and angular velocity (Fig. 8).

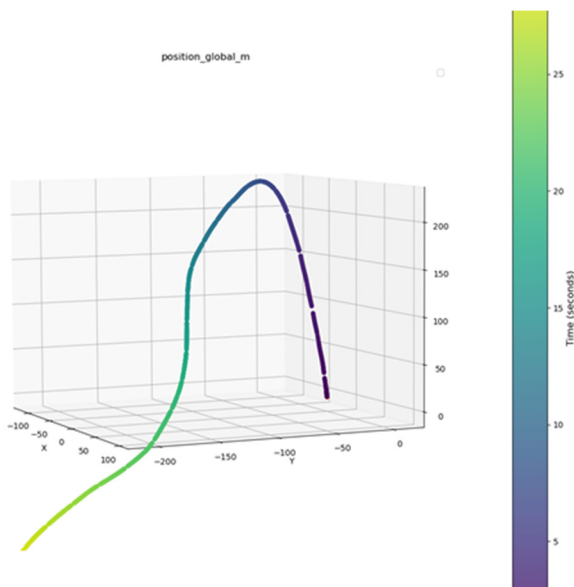


Figure 8: Bottom stage 3D flight path, recreated with IMU integration

The accuracy of the final path is debatable, however, due to integration drift. Further, the chaotic rotations after parachute deployment caused us to lose our orientation basis, which we tried to reset by assuming our stable descent acceleration vector was opposite to

gravity, which may not be the case when descending sideways. These theoretical concerns are practically shown in the IMU's path ending 150 m below the launch site and 650 m away, which is contradicted by eyewitness accounts.

All three sensors measuring the rocket's height (IMU, BME280 and GPS) agree that the rocket reached its apogee at around 220 – 235 m above ground, though the IMU suggests it reached it two seconds before the other two.

It is worth noting we reached the most logical results by aligning the BME's starting point to be at 0 m, but aligned the GPS based on its end point. This way, the BME's and GPS's trajectories aligned far better (Fig. 9).



Figure 9: Height plots from the IMU (yellow), BME280 (red) and GPS (purple)

Comparing our recorded data with the simulation, we expected an apogee of 347 m, around 120 m higher than recorded, and a peak vertical velocity of 94.5 m/s as opposed to our integrated peak of 64.1 m/s (Fig. 10).

We believe the discrepancy between the simulated and measured performance may be due to higher-than-expected air resistance or a more massive rocket than anticipated. Regrettably, we did not weigh the whole rocket prior to the first launch.

We have published all our raw data and plots online [19].

Since the first flight failed successfully, we decided to repeat the process, iterating on our failures the SpaceX way.



Figure 10: Velocity plots from the IMU (yellow) and BME (green)

5 In-between Flights

For the second flight, we had to decide what and how to improve the previous design.

5.1 Lower Stage

Most of the lower stage stayed unchanged. We only fixed the engine mount, which suffered some damage when the ejection charges opened the parachute. We 3D-printed a plate, which we attached to the top of the damaged engine mount to provide additional structural integrity.

We also replaced the parachute since it suffered a burn hole at the first launch.

We also changed the way we launched the rocket. The launch rod no longer goes through the lower stage. Instead, we made a droplet-shaped launch lug on the side of the

lower stage, similar to one that we had on the previous upper stage, only slightly larger.

5.2 Transition

We now opted to use LW-PLA for the transition part, as it is one of the largest and heaviest components on the rocket. As a result, the new part weighed 55 g instead of the previous 70 g, even though it was 20% larger.

We kept the decoupler combustion chamber as regular PLA to avoid compromising its structural stability.

5.3 Upper Stage

The upper stage needed to be rebuilt completely due to the motor explosion.

We also redesigned the upper fins according to the latest simulation (Fig. 11).

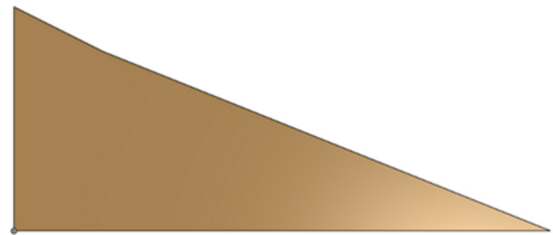


Figure 11: The new shape of the upper fins
We chose LW-PLA for the engine mount, too.

5.4 Nose Cone

We decided against using LW-PLA to move the rocket's center of mass, C_g , upwards for a more stable flight.

5.5 Electronics Improvements

We rebuilt the ignition mechanism from the ground up, utilizing two N-channel MOSFETs (AO3400A) instead of a relay. With this wiring, we also pulled an extra 250 mA directly from the batteries to help power the igniter. We switched to a 1 F supercapacitor, saving some battery charge and lowering the required charge time (Fig. 12).

Finally, we added a diode (1N5817) to prevent backpowering the batteries when the capacitor is charged to a higher voltage.

Extensive unit testing was done at several battery voltages to confirm this system to be incredibly reliable even in extreme situations (for example, a 3.3 V main battery voltage instead of the nominal 5 V).

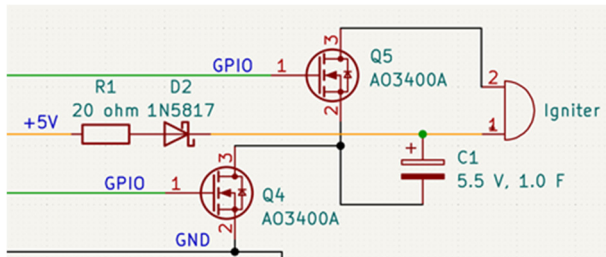


Figure 12: The new ignition system

We added a complementary launch detection mechanism: a wire which connects two GPIO pins together: the “source” pin is set to GPIO low, and the “drain” pin is pulled up to 3.3 V.

When the wire connects them, the drain pin will drop to GND. If the wire is then disconnected, the pin will once again rise to 3.3 V.

When the rocket begins its ascent, the wire is disconnected, which can be easily detected. It is important to note that we must also check if the wire is initially connected to avoid an early triggering.

We also switched the bottom stage IMU to be the ICM20948 as well, as it is purely an upgrade from the MPU6050, also simplifying our electronics to just one schematic for both stages.

5.6 Software Improvements

As a backup to the rather unreliable SD-card modules, we also implemented an automatic fallback by logging directly to the RPi Pico 2’s flash storage. It has about 4 MB of space available for our executable and logs.

In order to speed up writes, we always write full 256-byte sectors, and we pre-erase the entire flash before uploading our code [20].

We improved our live telemetry and communications capabilities. It is now possible to double-check the status of the controllers prior to launching the rocket and to remotely arm and disarm the launch mechanism.

We also hardened and improved the performance of the GPS NMEA parser, particularly to account for occasionally malformed data packets, and dropping them if they don’t contain valid data frames.

We also added two special startup modes, activated by grounding two pins on the microcontroller: one for charging the capacitor and one to dump the written flash.

6 Second Flight

We arranged for a second launch window on the 27th of August, between 9:00 and 11:00 AM, once again at the Poček training ground. We had some minor difficulties in the initial preparations of the rocket, which we attribute to its accelerated repairs and upgrades, as well as our nervousness.

The most significant consequence of this was rendering the bottom launch rod detector inoperable, as we could not properly reach its connector on the module after gluing the electronics compartment in place.

This was compounded by a separate issue: around a day before the flight, the IMU on the lower stage stopped working and no longer acknowledged any I2C communications. We double-checked all electrical connections and even added a backup MPU6050, which seemingly did not work either.

This meant that the lower stage now only had one of three possible functional launch detection mechanisms, though only one was ever needed to report a (false) positive to trigger a (false) launch.

As it turned out, this was exactly what happened. Immediately after the rocket was remotely armed, the lower stage’s BME280 falsely detected a large spike in vertical veloc-

ity, sending the upper stage into a nearby forest approximately three seconds later (Fig. 13).

The stage likely crash-landed before triggering the parachute ejection charge, meaning we could not receive any communications or identify any contrasting features. Regrettably, this caused us to be unsuccessful in locating what was left of the upper stage.



Figure 13: The surprised authors after an unexpected launch

6.1 Results of the Second Flight

We do not have any meaningful experimental data to interpret from this flight. However, it is still valuable to see what went wrong and how to prevent it next time.

We were able to reproduce the issue after the fact by running the module in fresh air, highlighting a core issue in our testing: we were only ever doing so in stale air.

Running the module close to real operating conditions revealed a bizarre pattern of readings (Fig. 14).

We found out, that the BME280 sensor reports sharp spikes, causing deltas as high as 8 m in only 240 ms, which is detected as a launch event in our code, designed to minimize latency between real events and detection.

We believe we should have relied on naturally lower-latency methods (IMU or launch rod wires) to detect liftoff. We find the BME280 to be useful in this application only as a last resort.



Figure 14: Height based on the BME280 pressure readings

For the next attempt, we plan to add checks to filter out broken launch detection mechanisms prior to arming the rocket, and believe this should have been a prerequisite for relying on those systems in the first place.

7 Discussion

We hope this paper provides useful insights into similar research, highlighting some possible pitfalls and important considerations. We hope we have shown the importance of end-to-end and unit testing, especially in real operating conditions.

We plan to continue our research and development until we reach a reusable, reliable, and accurate platform, learning from all our mistakes along the way.

Further, we plan to cooperate with the student aerospace group Noordung Labs [21] by providing them with experimental data, specifically for their navigational flight computer.

8 Conclusions

We have demonstrated that we were able to produce a mechanically flight-ready rocket twice, being limited only by electronic failures.

The first and second flights showed the flight capability of the lower and upper stages, respectively. In their aftermath, we have shown our ability to successfully diagnose and fix failures, as well as enrich and interpret experimental flight data.

There is much room for improvement in the process of detecting failures before the flight.

Our final conclusion is: Rocket science is hard and unforgiving.

9 Acknowledgments

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Finally, we would like to thank the Slovenian Armed Forces, particularly Lieutenant Colonel Peter Zvonc, for graciously providing a suitable launch site.

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Construction and Characterization of a Pirani Vacuum Gauge Based on an Incandescent Light Bulb

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Abstract: Across many industrial and technological processes, measuring the vacuum level is required for successful operation. Vacuum is assessed using vacuum gauges, one example of which are Pirani gauges. They are ubiquitous due to their simplicity and effectiveness for measuring pressure in the medium vacuum region. This article explores the feasibility of making a homemade Pirani vacuum gauge where the sensing element is made from an incandescent light bulb. The sensor is brought beyond the proof-of-concept level by designing a custom circuit board with a supporting power supply, analog front end and a microcontroller. Custom software was also developed to support sensor characterization by collecting, displaying and analyzing measurement data. The sensor was designed to be compatible with a standard KF16 vacuum connector system. With no access to gauge standards, the characterized sensor's readings were referenced against a commercial Pirani sensor. The developed sensor shows potential for use in vacuum measurement applications, though some unexplained issues remain, requiring further exploration.

Keywords: pressure measurement; vacuum gauge; Pirani vacuum gauge

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1 Introduction

The Pressure measurement is a common requirement in many different fields. It can be carried out using two main types of instruments: direct and indirect pressure gauges [1]. At higher pressures, direct gauges can be used as they rely on measuring the force exerted on a surface by incident particle flux [3] – [5]. Their readings are independent of gas nature [4]. However, as the pressure decreases, the force exerted becomes insignificant and reliable direct pressure measurement becomes impossible. In that range, indirect pressure gauges are required. They rely on detecting changes in gas

properties, often thermal conductivity, which behave predictably as the pressure changes, but are dependent on the nature of the gases in the monitored atmosphere [3] – [5].

In 1906, a German physicist named Marcello Pirani was the first to use the tungsten filament from a light bulb to measure pressure at a rough to medium vacuum range [2]. His invention has since proven indispensable in many industrial and scientific processes where such vacuum assessment is required [4].

Pirani's invention falls under the category of thermal conductivity gauges, which measure

thermal conduction of the surrounding gas [6]. A sensing element, often a tungsten wire, acting as a resistor, is attached to a vacuum chamber and connected to electricity. The wire's temperature increases until it reaches an equilibrium between the supplied electrical power (P_e) and the dissipated heat [4]. Heat dissipation occurs by thermal conduction of the gas, convection, radiation and thermal conduction through electrical leads [6]. The last two are pressure independent and thus considered parasitic. Together, they determine the maximum possible temperature and the lower limit of the measurement range [4]. In the higher region of the rough vacuum range convection is important for heat dissipation, however it becomes negligible at lower pressures as the number of direct collisions of particles with the walls exceeds the number of intermolecular collisions [4], [6]. The equilibrium is described by the following equation adapted from [4]:

$$P_e = \frac{U^2}{R} = RI^2 = \Lambda A \Delta T + h_c A \Delta T + \Re \lambda_c A \Delta T + \zeta_1 \sigma A (T_1^4 - T_2^4), \quad (1)$$

where A is the contact surface area, ΔT is the difference between the temperature of the heated element (T_1) and the temperature of the gauge housing (T_2), Λ is the coefficient of thermal conduction of a gas at high-vacuum, h_c is the heat transfer coefficient, $\Re$ is the geometric factor, λ_c is the coefficient of thermal conductivity of electrical leads, ζ_1 is the material emissivity coefficient of the wire surface, and σ is the Stefan-Boltzmann constant.

Since the temperature coefficient of resistance (α) for metals holds a positive value [4], the increase in resistance can be related to a decrease in thermal conduction of the gas when the supply of electrical energy is constant. Dependent electrical quantities may also be measured and their changes related to changes in resistance. The relationship is described by the following equation:

$$R_2 = R_1 [1 + \alpha(T_2 - T_1)] \quad (2)$$

where R_2 represents the resistance at temperature T_2 and R_1 the initial resistance at the initial temperature T_1 .

Thermal conduction of the gas is a function of the number of particle collisions with the wire [6] and increases proportionally with pressure. As the pressure and thus thermal conduction of the gas decreases, so does the filament cooling. This causes an increase both in the wire's temperature and resistance. Considering all of this, resistance can be related to pressure through temperature.

1.1 Implementation

Traditionally, the sensing element of a Pirani gauge (R_p) was used as an arm of a Wheatstone bridge [3], [4], as shown in Figure 1. A variable resistor (R_2) was then used to balance the bridge. Another wire was placed in an evacuated and sealed off tube (R_c) to help correct for temperature induced changes [3]. The bridge was then used to detect changes in resistance. Modern electronics allow us to skip the tedious process of manually balancing the bridge, or replace it altogether with a more precise analog to digital converter.

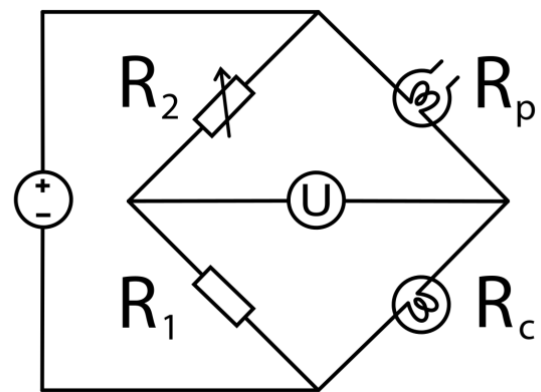


Figure 1: A diagram of a Wheatstone bridge used in a traditional Pirani vacuum gauge.

A Pirani gauge can be operated in three modes: constant voltage, constant current and constant resistance, sometimes referred to as the constant temperature mode. In the first two modes, a known voltage or current is

applied to the sensing element, and the other quantity is monitored to calculate the resistance. In either mode, the calculated resistance of the sensing element is used to determine the monitored pressure [6]. In constant resistance mode, a controller continuously monitors both the voltage and the current. The excitation power is adjusted so that the resistance is kept constant, and the pressure is calculated based on the supplied power [3]. Although the constant temperature mode is the most precise, constant current and constant voltage modes are commonly used due to their simplicity [3].

When talking about a vacuum gauge, the important qualities to consider are its range, sensitivity, selectivity, magnitude and character of effect on the pressure measurement. A Pirani vacuum gauge's range may span from rough to medium vacuum ($10^3 \text{ torr} - 10^{-4} \text{ torr}$), depending on the construction and geometry of the gauge [4]. It offers quick and precise detection of small changes in pressure, however, the sensitivity may vary depending on the mode of operation that is being used [3]. A Pirani gauge does not significantly disrupt or change the actual pressure or the measurement itself [4]. It can be used for different gases, but calibration curves should be applied to correct for differences between the indicated and actual pressure [3].

Nowadays, Pirani type vacuum gauges no longer use light bulb filaments. The sensing elements are more often than not custom made. In this paper, we take one step back and design and characterize a custom lightbulb-based Pirani vacuum gauge, albeit with modern electronics.

2 Materials and Methods

In this section, the construction of our gauge, as well as the initial testing setup are presented. Each individual part is described in more detail in its respective subchapter, but a quick overview is provided first.

The gauge was designed to be compatible with the standard KF connector system. Two incandescent light bulbs were integrated into a KF16 flange cap. This allows for fast and secure connection to a vacuum system. The lightbulb leads were soldered onto a printed circuit board (PCB). A photo of a Pirani sensor prepared in this way is shown in Figure 2. It should be noted that while the PCB has two analogue front end (AFE) channels, only one was populated with components, as the scope of this article did not require both.

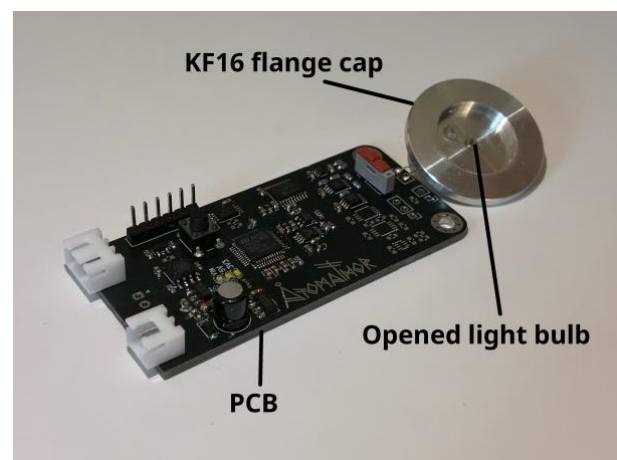


Figure 2: The bulb leads soldered onto the PCB.

2.1 The sensing element

In our experiments, generic tungsten-filament light bulbs with a diameter of 3 mm and a nominal voltage of 24 V were used. A 24 V model was selected over the lower voltage variants for its higher nominal filament resistance, 80Ω in this case. This leads to higher absolute change in resistance for the same change in temperature. The light bulbs were glued into an aluminum flange cap using an epoxy glue, UHU article number 63017. For better adhesion, the light bulbs were first sanded using a 400 grit sandpaper. To expose the filaments to chamber conditions, the casings of the light bulbs were sanded down to create an opening, once again utilizing the aforementioned sandpaper. The light bulbs in their (a) unmodified, (b) sanded, and (c) opened up form are shown in Figure 3.

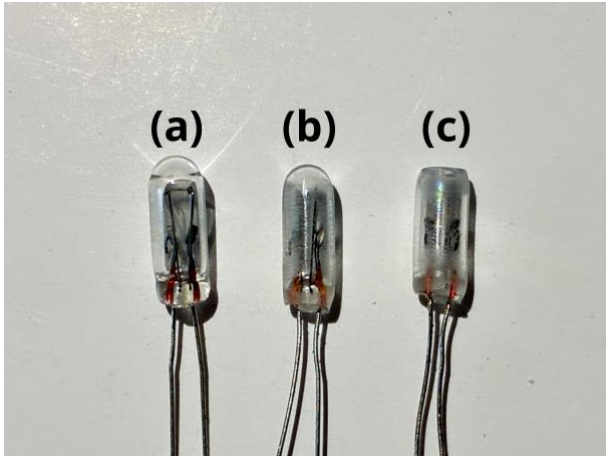


Figure 3: Light bulbs in their (a) unmodified, (b) sanded, and (c) opened up form.

It should be noted that the light bulbs' leads were very prone to breaking. To mitigate the problem, a soft wire was soldered to the leads, and the connection was then immobilized with more epoxy glue, which solved the problem.

2.2 Experimental setup

Indirect pressure gauges are typically calibrated with direct pressure gauges (primary standards). The empirical approach is preferred over mathematically deriving equations due to the complex nature of relationships between the measured properties and pressure. In part of the high-vacuum region, where direct pressure gauges fail, secondary standards (indirect pressure gauges), which had been calibrated using primary standards, can be used to calibrate other indirect vacuum gauges creating working standards [4].

With no access to gauge standards or calibrated references, our gauge was calibrated against a commercially available Pirani type vacuum gauge, which also contains a cold-cathode inverted-magnetron gauge, a PKR 361 from Pfeiffer Vacuum, with no known calibration certificate.

It should also be noted that the commercially available PKR 361 gauge provides the pressure measurement as an analogue voltage between 0 V and 10 V. It was monitored using a voltage divider made from generic resistors

and an ADC1115 ADC from Texas Instruments, which may incur additional pressure measurement errors, offset, and drift.

The calibration was done by connecting both our gauge and the commercial one to a vacuum chamber. The vacuum was drawn by a DUO 1.6 dual stage rotary vane pump from Pfeiffer Vacuum, and a VB M-B vent valve from Vacuubrand with a generic needle valve as a flow restrictor was used to vent the chamber afterwards. The schematic of the setup is shown in Figure 4. The pressure was cycled repeatedly while being monitored and recorded, along with the current and voltage across our gauge, using the custom software described in Section 2.4. Our sensor was operated in constant voltage mode set to 0.1 V, 0.5 V and 1.0 V.

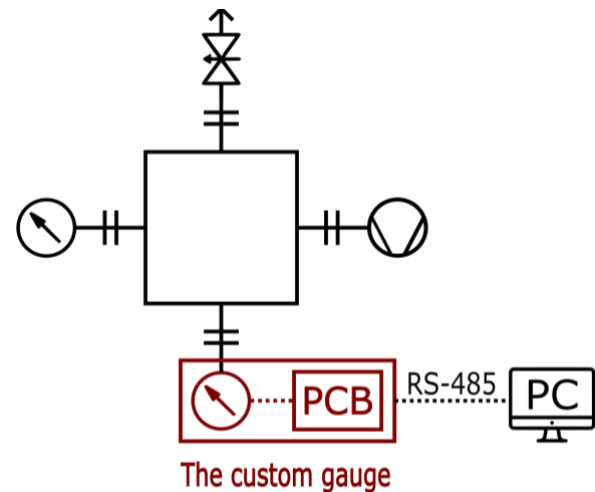


Figure 4: A schematic diagram of the testing setup with the custom gauge marked in red.

2.3 Description of the PCB

To measure the voltage and current on a Pirani bulb, a PCB was designed. The PCB integrates the complete AFE, digital control, power management and communication interfaces required for operation of the gauge.

The PCB was designed such that constant voltage and constant current modes of operation are supported. Additionally, constant resistance mode can be achieved with software support. They are described in more detail later in this section.

The block diagram of the developed PCB is shown in Figure 5. An STM32G051C8T6 microcontroller from ST Microelectronics was used for controlling the system and coordinating the measurement process. It communicates with a digital to analog converter (DAC) and an analog to digital converter (ADC), controls the excitation circuitry and collects the measurement data, as well as transmits the acquired values through an RS-485 interface.

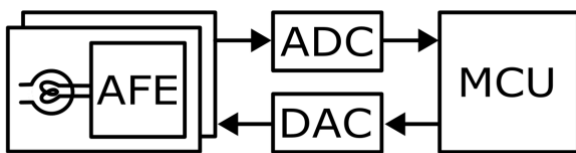


Figure 5: A block diagram of the developed PCB.

For constant voltage mode, the reference voltage is generated by DAC8551, a 16 bit DAC, and buffered with TLV2888, a high precision zero drift operational amplifier both from Texas Instruments. A dedicated 2.5 V voltage reference, MCP1501 from Microchip Technology, is used.

Constant current mode is achieved using a Howland current pump as proposed in [7]. This setup converts a control voltage into a defined output current. The current is primarily determined by the applied control voltage and the accurately matched resistors. The DAC that controls the voltage in the constant voltage mode is reused for controlling the current source, with an additional operational amplifier of the same model. To minimize current fluctuations, offset related errors and long term drift, high precision 0.1% offset, 25 ppm/K drift thick film resistors were selected.

The voltage across the Pirani bulb is measured directly using MCP3564, a 24 bit delta sigma differential ADC from Microchip Technology. The filament voltage is measured differentially to minimize the contribution of the ground plane resistance. The high resolution ADC was chosen to eliminate the

need for a Wheatstone bridge setup to detect small changes in filament resistance. The current through the bulb is measured on another channel of the same ADC, using an INA190A1 current sense amplifier from Texas Instruments, in combination with a precision 10 Ω shunt resistor.

For parallel testing, the PCB was designed to facilitate the simultaneous measurement of two Pirani bulbs. Each bulb is provided with its own excitation and measurement path, allowing two sensing elements to be operated and characterized under the same experimental conditions. The operating mode of each bulb can be selected manually using a dedicated switch on the PCB, allowing the user to independently select either constant voltage or constant current excitation for each sensing element. This provides additional flexibility during testing and makes it possible to compare the two measurement modes in parallel, using identical environmental and vacuum conditions. Certain components are reused across multiple modes to reduce the number of components and save on cost.

The PCB was designed as a four-layer board primarily to simplify the layout and improve the overall organization of the circuitry. The structure consists of a top signal layer, two internal layers used primarily for power and ground distribution, and a bottom signal layer. This arrangement provided a convenient way to organize the different circuit sections while maintaining a compact and manageable PCB layout.

2.4 Software

The software consists of two parts: the firmware running on the microcontroller and a desktop application, which performs processing on the raw data provided by the microcontroller and displays it on real-time graphs. The ADC is configured to continuously measure the voltage and current channels. The measurements are timestamped by the MCU and provided to the desktop application

when polled. The desktop application aggregates the voltage, current and pressure values by averaging them in 0.5 s intervals, which allows for graphing the values in relation to each-other as well as time. After the experiment is complete, the collected data can be saved in a simple CSV file, allowing further processing and analysis using scripts or off-the-shelf software.

3 Results and Discussion

Multiple experiments were conducted on the designed Pirani gauge using the constant voltage method. Data was collected at multiple voltages, specifically 0.1 V, 0.5 V and 1 V. Each measurement consisted of pumping the system down as low as our vacuum pump allowed, approximately 20 μbar , before venting back to atmospheric pressure. The results of each individual set of tests are shown in Figures 6, 7 and 8. On the x-axis is the pressure indicated by the PKR 361 reference vacuum gauge, while the y-axis shows the resistance calculated using the measured voltage and current through the light bulb filament.

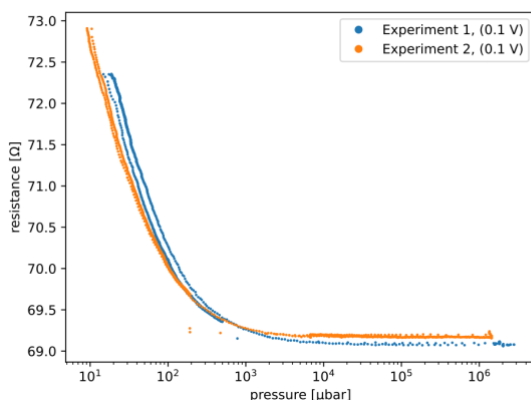


Figure 6: Experiment results at 0.1 V.

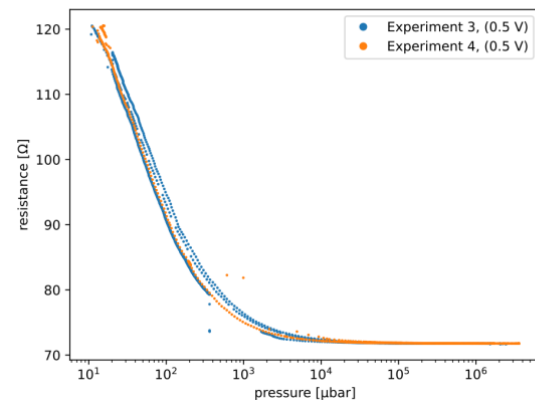


Figure 7: Experiment results at 0.5 V.

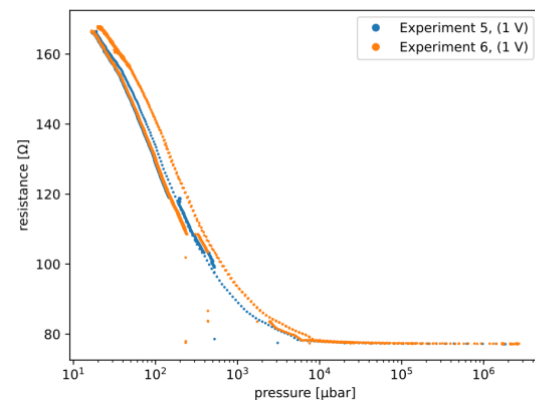


Figure 8: Experiment results at 1 V.

In Figure 9, the measurements at all three set voltages are shown together. It can be observed that the measurement range shifts based on the applied voltage. Higher voltages improve the range at higher pressures, while lower voltages extend it to lower pressures. The former can be attributed to better heat transfer that occurs as a result of a greater temperature gradient. The latter may be a result of heat dissipation through gas interactions becoming negligible in comparison to heat dissipation due to thermal conduction through electrical leads. This is visible in Figure 9 at lower pressure where the graph begins to level off.

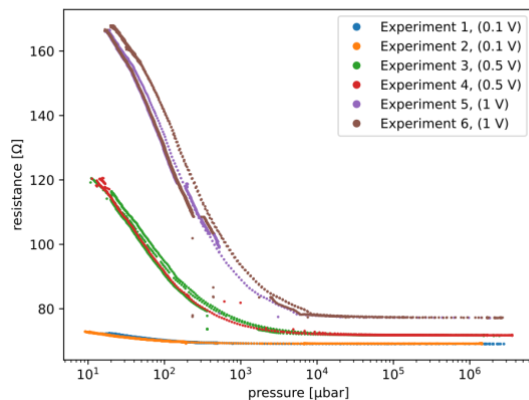


Figure 9: Measurement results at all three set voltages.

The 0.5 V and 1 V sets show considerable drift during the pumping and venting parts of cycles. This may be a result of thermal inertia when the chamber is vented too quickly, considering the drifting curves converge closer to atmospheric pressure when the venting speed decreases. Various resources indicate hysteresis is possible [8], however, an extensive analysis of the phenomena is beyond the scope of this work.

4 Conclusion

A low-cost Pirani-type vacuum gauge based on an incandescent light bulb was shown to be feasible. Our measurements show clear correlation between sensor readings and the chamber pressure. Based on these findings, we intend to continue our work to develop a fully functional pressure gauge. There are multiple possibilities for future improvement. To minimize the effect of lead resistance, four wire voltage measurement could be implemented. Furthermore, this paper only focused on operating the sensor in constant voltage mode. Implementing a constant resistance mode could improve the accuracy, while constant current mode could make it easier to compensate for voltage drop on sensor leads. Finally, sensor hysteresis could be analyzed in more detail if pumping and venting speed could be controlled accurately, which our currently available vacuum system does not allow for. We hope to resolve the

issue in the near future and continue the work on developing the sensors.

5 Acknowledgments

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Design and Development of a Thermal Evaporation System for Metal Thin Film Deposition

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Abstract: Physical vapor deposition (PVD) is a widely used technique for depositing thin layers of materials onto a substrate. Thermal evaporation is a prominent example of a PVD technique. This article describes the development of a system suitable for this process. The design includes a custom vacuum chamber, a high current electrical pass-through, and a vacuum pump system. The main component is a vacuum chamber, designed around a glass tube, that integrates all required connectors for atmosphere control. To achieve the required vacuum, a turbomolecular pump is used in conjunction with a two-stage rotary vane roughing pump. The vacuum level is monitored with a combined Pirani and cold-cathode inverted vacuum gauge. The bottom cover includes a KF50 flange for a thermal evaporation module, which consists of aluminum feedthroughs and the evaporation boat. These feedthroughs connect the boat to the switching power supply unit, allowing the electrical current and voltage to be limited. To control the thermal evaporation process, a custom set of electronics and software was designed. Together, they allow us to monitor and log system parameters such as pressure and the evaporation boat heating current. We successfully developed and designed a system for depositing thin films using the thermal evaporation method, along with some expansion ports to allow the addition of magnetron sputtering capabilities in the future. Although construction of the system is not fully finished, some components have already been made and are shown in this article.

Keywords: thin-film; thermal evaporation; heating boat

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1 Introduction

Thin-film deposition is an atomic deposition process in which a layer of material in thickness ranges of a few nanometers to about ten micrometers is applied onto the substrate [1, p. 14]. This process is usually

used to improve the desired properties of a surface. One of the most prominent methods of thin film deposition is physical vapor deposition (PVD) [2, p. 2720].

1.1 Physical vapor deposition

There are different PVD methods, all of which can be broken down into three main steps: vaporization of the material, subsequent vapor transport, and ultimately condensation of the vapor onto a substrate. Two of the more prominent PVD methods are thermal evaporation and sputtering. We explored the latter in our previous work [3], and this year we tackled the design of a system for thermal evaporation that is also compatible with the sputtering module from the aforementioned work.

1.2 History

In the late nineteenth century, a phenomenon of bulb blackening was observed in incandescent light bulbs, which was later found to be caused by evaporation of the filament [4, p. 130].

Thermal evaporation experienced very little adoption until John Strong invented the first method for aluminizing mirrors by vacuum evaporation of aluminum. It should be noted that aluminum was one of the materials that was difficult to electroplate [5, p. 37].

1.3 Overview of thermal evaporation

The three main stages of the thermal evaporation process, which are numbered consecutively, take place inside a vacuum chamber and are shown in Figure 1. In stage 1 the material is placed on the heating element, where it evaporates. In stage 2 the resulting vapor is transported through high vacuum, and in stage 3 it is deposited onto the substrate. Because the source material evaporates as individual molecules or atoms and not as larger particles, a thin-film coating can be obtained [6, pp. 2–3].

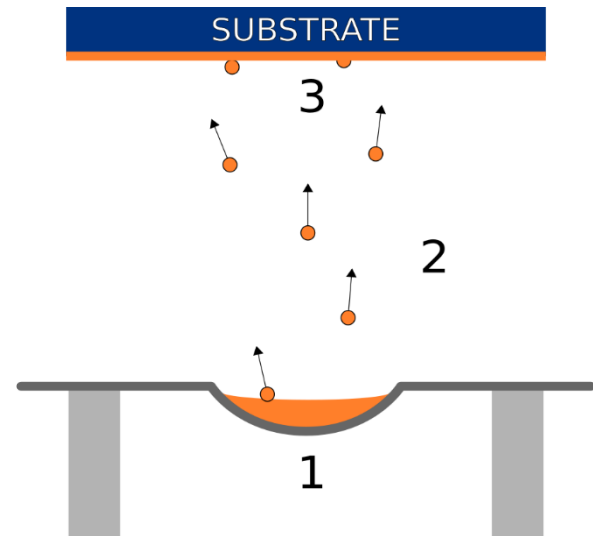


Figure 1: The basic overview of the thermal evaporation process. Stage 1 presents evaporation of the material, stage 2 vapor transport through vacuum and stage 3 material deposition onto the substrate.

1.4 Material source

There are two common methods for heating a material to its boiling or sublimation point. The first is electron beam evaporation, in which the material is evaporated by directing an electron beam onto the target. This method is best suited for materials with high melting points [2, p. 2950]. The second method is resistive heating, which is much simpler from a technical point of view. In this method, electrical current passes through a resistive heating element commonly referred to as a “heating boat” or simply a “boat”. It is usually made of tungsten, tantalum, or molybdenum, because these materials are well suited for high temperature applications [6, pp. 53, 82].

The heating power is proportional to the boat’s resistance and to the square of the applied current, as described in Equation (0) [6, p. 82].

$$P = I^2 R(T) \quad (0)$$

It should be noted that the heating element's resistance depends on its temperature.

The evaporation temperature of materials changes with pressure. In a vacuum, most materials evaporate at lower temperatures than they do at higher pressures. Materials evaporate when the surrounding pressure equals the vapor pressure, which increases with temperature. The relationship between vapor pressure (p) and temperature (T) is given by Equation (1) [7],

$$\log_{10} p = A + \frac{B}{T} + C \cdot \log_{10} T + D \cdot T \cdot 10^{-3} \quad (1)$$

where pressure is given in atmospheres and temperature in kelvins. The parameters A through D are listed in the literature for each metal and vary based on their state of matter. This means that some materials, which may seem difficult to evaporate at standard temperature and pressure, may be easier to evaporate in high vacuum conditions.

The relationship between vapor pressure and temperature for several metals is shown in Figure 2.

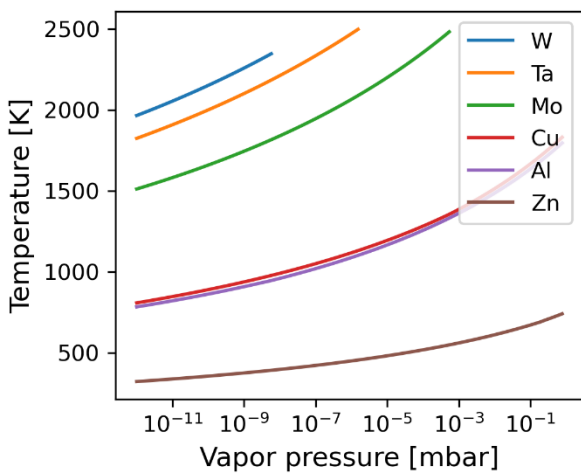


Figure 2: Relationship between vapor pressure and temperature for certain metals according to the equation from [7].

1.5 Vapor transport

When vapor emitted from the source travels to the substrate, it might collide with residual air molecules. This would result in it losing momentum and reducing the likelihood of reaching the substrate. To minimize this unfavorable effect, the mean free path inside the chamber should ideally be larger than the distance between the boat and the substrate. The mean free path (l) is defined as the average distance traveled by a particle before colliding with another particle [6, pp. 23–25]. It is inversely proportional to the pressure (p) and is calculated using Equation (2) [8, pp. 6–65],

$$l = \frac{k T}{\sqrt{2} \pi a^2 p} \quad (2)$$

where k is the Boltzmann constant, T is the temperature in kelvin, and a is the effective collision diameter of gas molecules. The gas is assumed to behave as an ideal gas. The correlation between mean free path (l) and pressure for argon, where the effective collision diameter is 0.358 nm [8, pp. 6–65], is presented in Figure 3.

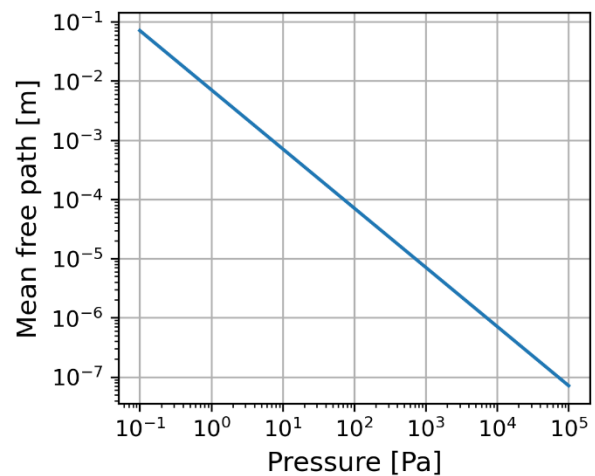


Figure 3: Mean free path as a function of pressure according to Equation (2), assuming an effective collision diameter of 0.358 nm.

The ratio of mean free path to the distance between the source and the substrate (L), $Kn = l/L$, is called the Knudsen number. Systems with $Kn > 1$ are desirable because most vapor particles will not encounter any residual air particles on their way to the substrate [6, p. 94].

1.6 Thin-Film Deposition

When an incoming particle approaches the substrate surface within a few atomic distances, it begins interacting with it via van der Waals forces. The particle accelerates toward the surface as it is drawn into the potential well. At a certain distance from the surface, it is decelerated by repulsion from the other nuclei. If this interaction dissipates enough momentum perpendicular to the surface, the particle weakly bonds to the substrate through physical adsorption. From that state, it can move along the surface, desorb, or chemically adsorb, forming a stronger, more permanent bond [6, pp. 120, 121].

1.7 Vacuum compatible materials

Some materials may evolve gases and vapors when put in vacuum, which is known as outgassing. Therefore, materials used in vacuum systems must be chosen carefully to minimize contamination. For example, zinc, because of its high vapor pressure, outgasses and is thus not suitable for use in high vacuum. The preferred material for constructing vacuum chambers and other vacuum components is stainless steel. Aluminum alloys are also appropriate if subjected to the right surface treatment [6, pp. 50–53].

The joints between components must be sealed properly to allow the system to reach high vacuum. Elastomers are well suited for this purpose because of their

ability to conform to surface irregularities. Some elastomers are prone to outgassing or are susceptible to gas permeation and are thus incompatible with high vacuum [6, p. 52], [9, p. 321].

1.8 Aim of this work

Our goal for this project was to design a highly versatile vacuum system for thin-film deposition that can also support a range of different vacuum experiments.

2 Materials and Methods

In the previous section, the basic underlying principles and constraints of the thermal evaporation process were presented, whereas this chapter focuses on our technical solutions.

2.1 Overview of the evaporation system

The presented system builds on our previous work, where a compatible sputtering module was described [3]. The main functional upgrades are more precise atmosphere control and the ability to coat a substrate through thermal evaporation. The main chamber assembly comprises a glass cylinder and an aluminum interface block with multiple KF connectors. The bottom lid facilitates an electrical passthrough for a thermal evaporation module. The entire system is mounted on a custom construction made of aluminum extrusions. Vacuum is maintained using a turbomolecular pump with a roughing fore pump. Each subsystem is described in more detail in its respective subchapter.

2.2 Chamber construction

The cross-section of the vacuum chamber assembly alongside the evaporation module is shown in Figure 4. The vacuum chamber is designed around a 200 mm tall borosilicate glass tube with an outer diameter of 150 mm and 7 mm thick walls. Custom seals were cut from a 2 mm thick fluoroelastomer (FKM) rubber sheet from Dihta. The glass tube sits on an interface block that includes all the required KF flanges. They were secured to the base tube with vacuum grade Hysol 1C epoxy from Loctite. The finished interface block is shown in Figure 5. The bottom cover of the interface block has a KF50 flange, designed to connect to the thermal evaporation module.

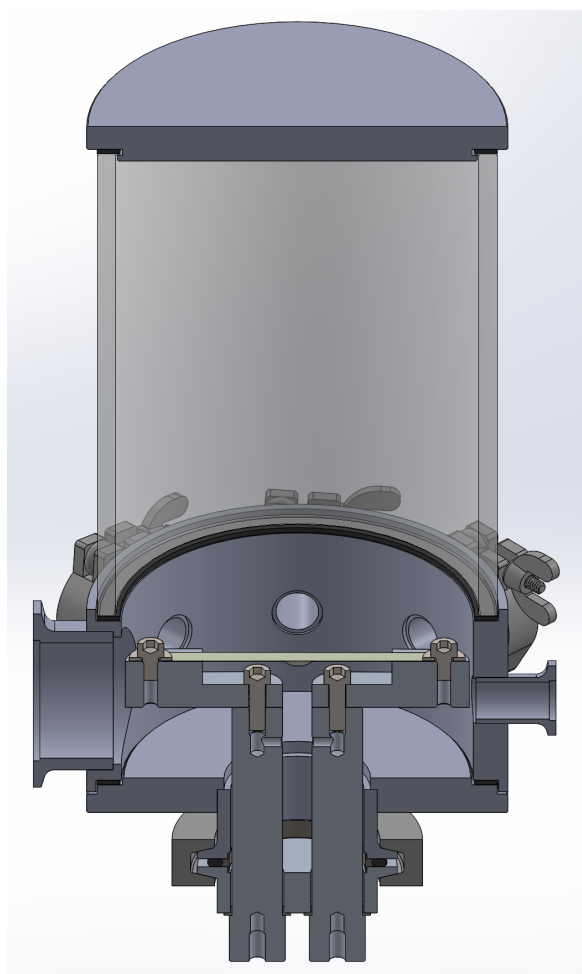


Figure 4: The vacuum chamber assembly cross-section.



Figure 5: The finished aluminum interface block with mounted KF flanges.

2.3 The vacuum system

The vacuum system is schematically presented in Figure 6. The chamber can be pumped down using either only a roughing pump or the roughing pump in conjunction with a turbomolecular pump. These are Duo 1.6 and SplitFlow 80 respectively, both from Pfeiffer Vacuum. The pumps and the chamber are connected through metal bellows with KF flanges. The roughing pump is connected through 24.5 series KF16 inline valves from VAT Vacuum. To achieve greater pumping speed, the valve between the turbomolecular pump and the chamber is a larger 01.2 series KF50 gate valve, also from VAT Vacuum.

The pump-down process is a standard procedure for systems with individually isolatable roughing and high-vacuum pumps, as described in [10, p. 74].

The pressure inside the chamber is monitored using Pfeiffer Vacuum's PKR 360 vacuum gauge, which integrates both Pirani and cold cathode gauges. It can measure pressures down to 10^{-9} mbar. An auxiliary pressure system monitors the performance of the backing pump when the turbomolecular pump is running. That sensor is a

TPR-250 Pirani vacuum gauge from Balzers. Since both sensors provide readings as analog electrical signals, a custom printed circuit board (PCB) for digitizing the readings was made. The computer communicates with the PCB through an RS-485 interface. The force holding the chamber's top and bottom lids shut is estimated to be around 1500 N at 1 mbar. Opening the chamber therefore requires equalizing the internal pressure with the surrounding atmosphere. This is done through a VB M-B vent valve from Vacuubrand. For future expandability, some additional KF16 connectors were left unused.

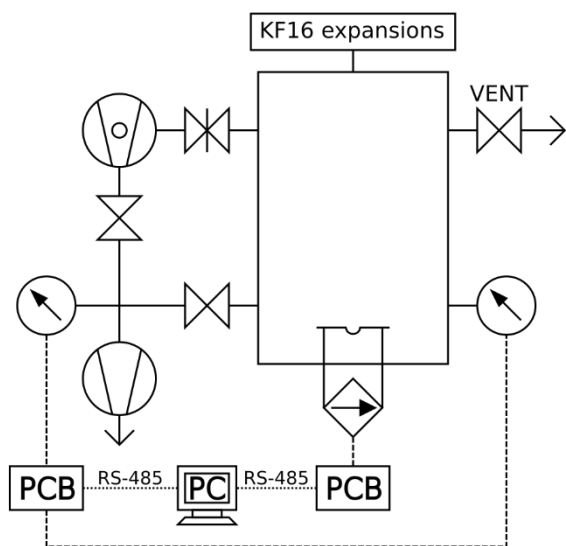


Figure 6: Schematic diagram of the vacuum system configured for thermal evaporation.

2.4 The evaporation module

The constructed evaporation module is shown in Figure 7. It attaches to the main chamber assembly through a KF50 flange at the bottom. The two high current aluminum feedthroughs are attached to the flange with vacuum grade Hysol 1C epoxy from Loctite. The boat is fastened to the supports with a pair of bolts and washers.

To facilitate the use of a wide variety of boats, interchangeable mounting blocks were envisioned. Those and the bolts are not present in Figure 7 but can be seen in the system cross section in Figure 4. A 0.13 mm thick S9A tungsten boat from Micro to Nano was chosen, and all dimensions were selected to facilitate its use. This model was chosen primarily for its comparatively lower price.

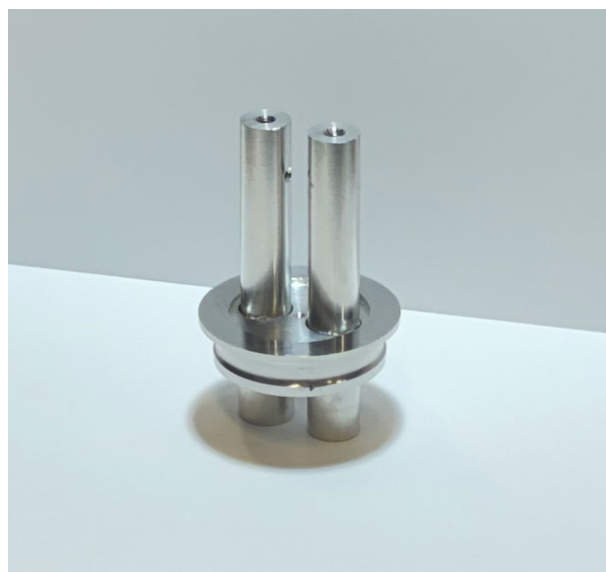


Figure 7: Evaporation module mounted on KF50 flange with two aluminum feedthroughs for connecting evaporation boat and power supply unit.

2.5 Boat-heating power supply unit

To provide power to the heating boat, a white label Chinese power supply unit (PSU) was used. The same or similar models are sold under many names and by many suppliers. Ours was a ZX-2000 from ZJIVNV, chosen because it was the most affordable. The PSU can output 12 VDC and up to 166 A. Both voltage and current can be limited through analog control, therefore, another custom PCB was made. It is powered by an STM32G051C8T6, a microcontroller from ST Microelectronics. In addition to generat-

ing the control signals, the PCB also receives and parses commands sent over an RS-485 protocol from a computer. The code running on the microcontroller was written in the C programming language and implements all necessary functionalities for operation of the evaporation system.

2.6 Boat simulation

As a rough estimate of what to expect, the heating of the tungsten boat at different electrical currents was simulated, and the results are shown in Figure 8. The heating due to resistive losses in the boat is described by Equation (0).

The electrical resistivity of materials changes with temperature. The numerical model describing the relationship between tungsten's resistivity and temperature was found experimentally and can be seen in Equation (3) below:

$$\rho = -2.72907 + 0.02585 \cdot T + 1.8971 \cdot 10^{-6} \cdot T^2 \quad (3)$$

where ρ is the resistivity of tungsten in $\mu\Omega cm$ and T is the temperature in kelvin [11, p. 95].

The simulation accounted for heat loss through radiation and thermal conduction through the aluminum support pillars, assuming a constant ambient room temperature at the ends of the support pillars and at the walls of the vacuum chamber.

The radiation was calculated using the following Equation (4):

$$P = \sigma \varepsilon A \cdot (T^4 - T_0^4) \quad (4)$$

where σ is the Stefan-Boltzmann constant, epsilon the emissivity, A the area, T the

temperature of the boat, and T_0 the temperature of the chamber. The emissivity of tungsten was calculated by Equation (5):

$$\varepsilon = (-2.6875 \cdot 10^{-2}) + (1.819696 \cdot 10^{-4}) \cdot T - (2.1946163 \cdot 10^{-8}) \cdot T^2 \quad (5)$$

This equation was fitted to experimental data and requires that the temperature is in kelvin [12, p. 38].

The thermal conduction through the supports was calculated using Equation (6):

$$P = \frac{k \cdot (T - T_0) \cdot A}{s} \quad (6)$$

where k is the thermal conductivity coefficient for aluminum, A is the heat transfer area, s is the thickness of the supports, T is the temperature of the evaporation boat, and T_0 is the outside temperature [13, p. 515.]

We decided not to calculate the temperature change of the supports caused by heat generated from resistive losses, since aluminum's resistivity is too low for it to make a noticeable difference.

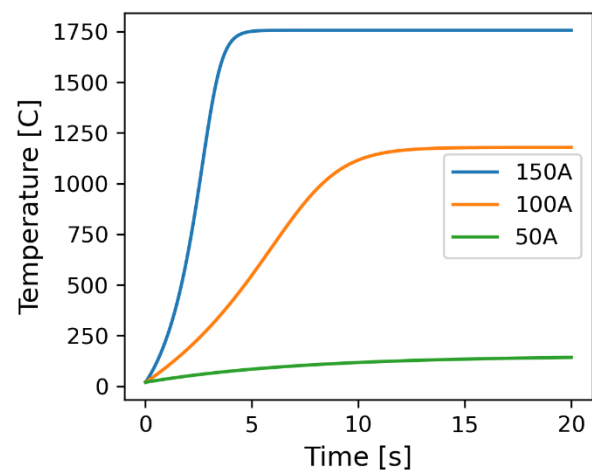


Figure 8: The simulated boat temperature over time when heating with different currents. The simulation was created using simplified equations.

2.7 Aluminum stand

A custom stand shown in Figure 9 was made from aluminum extrusions and designed to accommodate all the components required for evaporation. In addition to housing all the aforementioned components, it also includes a DIN rail for the circuitry and a space for pneumatics to drive the KF50 gate vacuum valve. To increase compactness, the system relies on external mains power and compressed air. The backing pump is located outside the main system for convenience and ease of transport, unlike the turbomolecular pump, which is mounted directly to the profiles.

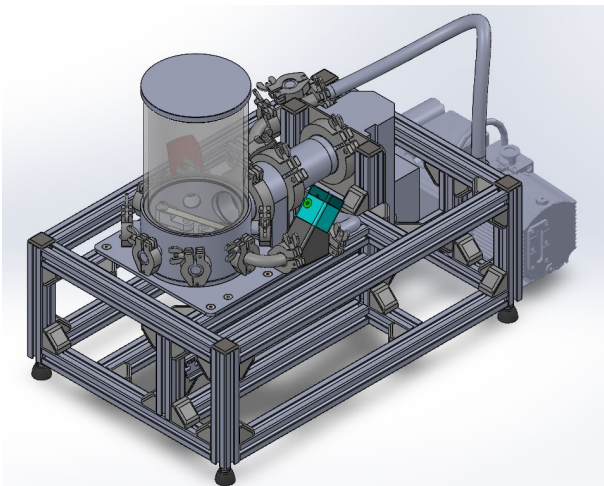


Figure 9: Assembly of the vacuum system configured for thermal evaporation.

3 Conclusions

We designed a modular vacuum system for thermal evaporation that can also be used for other vacuum-based processes. Most of the subsystems were constructed and tested separately. Custom PCBs were designed and programmed to control the main PSU and monitor the primary and secondary vacuum gauges.

In the future, we plan to integrate all subsystems into a fully functional thermal evaporation system. A precise atmosphere-

control system using mass flow controllers is planned to facilitate the magnetron sputtering module [3], which will be reworked to improve deposition rate and quality. The complete system will enable thin-film deposition with higher film purity and more accurate process control.

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Mastering the Curve: Hands-on Approach to Unreal Engine and VR Development

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Abstract: Unreal Engine is a well-known, cutting-edge software for developing games, simulations, training scenarios, multimedia, and movie special effects developed by Epic Games in 1995 and released 3 years later. The first commercial video game using Unreal Engine is Unreal, released in 1998. In this paper, the authors evaluate their own Unreal Engine learning process based on several years of practical experience in game and virtual reality development, and the approach they took when educating and helping younger peers master the engine. The authors have been learning Unreal Engine since primary school and during high school. Particular attention is given to challenges encountered by beginners, factors contributing to the engine's steep learning curve and strategies that may facilitate more effective skill acquisition. For this purpose, the paper also examines selected core features of Unreal Engine 5, including Blueprints, level design, user interfaces, materials and networking. Key features that are generally considered essential during the early stages of learning are also identified and their practical role in the development workflow is discussed. Finally, several student-developed projects are presented as case studies illustrating the practical application of acquired knowledge.

Keywords: Unreal Engine; learning curve; game development; game engine

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1 Introduction

Unreal Engine is well-known, cutting-edge software which is gaining more popularity every day. The software supports the development of games, making simulations, multimedia, movie special effects, architecture and more. It has been used in movies such as *The Mandalorian*, games like *Ark: Survival Ascended*, the *Mass Effect* trilogy, *Subnautica 2*, *Fortnite* and numerous others. Learning Unreal Engine (or any other game engine for that matter) to make a game that could be informative as well as fun to play and would feel like a finished game, is an inviting challenge for every beginner.

2 Starting with Unreal Engine

All projects and workflows described were developed using Unreal Engine 5 on Windows.

Since Unreal Engine is a fast-evolving development framework, it does not have a lot of stable documentation.

Therefore, one needs to rely on content creators that have made some tutorials using the same engine version, other people who have experience with this software, and the small amount of updated documentation that exists.

When opening Unreal Engine for the first time, one is greeted with several templates

and options and has to choose a starting template (Fig. 1).

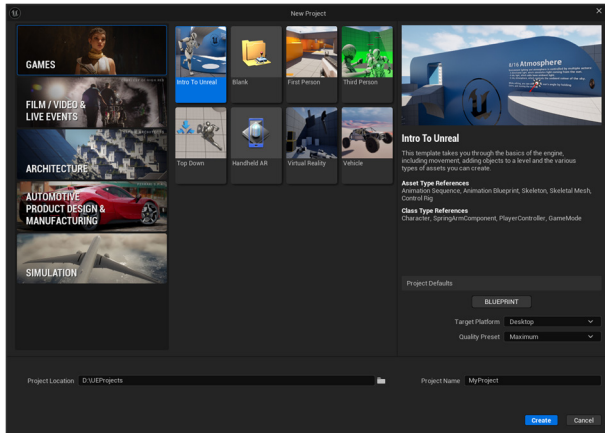


Figure 1: Template options

The templates have some initial code and assets that let a new user jump right into making gameplay without losing time and figuring out how to implement movement and other common functionalities. One can also start with a completely blank project.

For beginners, this is a welcome feature, since they are able to choose from templates such as first-person and third-person games, virtual and augmented reality, and several other types of projects, allowing for a fast start to developing.

After some time, when they are accustomed to the engine's environment, they can pick a blank template, allowing them greater control over the environment.

3 Unreal Engine Fundamentals

For a successful start, one needs to learn some ground basics.

3.1 Integrated development environment

Before making games, it proved useful to get accustomed to the Integrated development environment (IDE) first. The IDE consists of a viewport (Fig. 2), the detail tab, the outliner, the content browser, and several other panels

which are allowed to be reorganized according to a programmer's workflow.

For beginners, the default setup is generally good enough, since it is also used by the majority of online tutorials.

The editor is separated into smaller windows, each having its function. The beginner should get used to at least 4 windows.

The most important is the viewport, which is also the window on which the programmer can preview his work in a game-like environment. It is also used for placing, moving, rotating and scaling objects.

The properties of an object activated in the viewport can be changed in the details tab.

The hierarchy of the whole scene can be accessed and manipulated in the outliner tab.

The items that can be added to the game are called assets and are visible in the Content Browser. The Content Browser is an explorer-like window with assets that can be imported or created in the editor.

It is advisable for a beginner to follow established rules on how to organize the workspace, assets, naming conventions, etc., especially when collaborating with other developers. That way more people can work on a project with less friction.

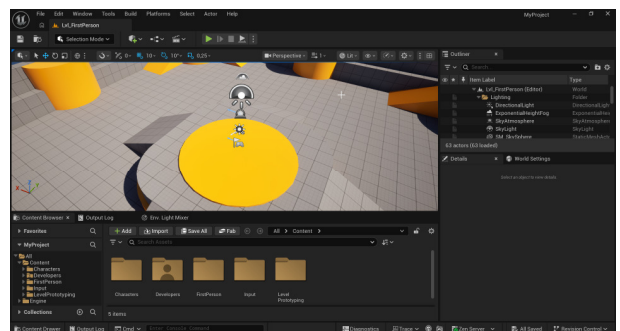


Figure 2: Viewport

The next smart step is to learn at least a few more common keyboard shortcuts, the window manipulation and general terminology (for example, every actionable item on the scene is called an actor).

3.2 Blueprints

One of the most important features of the Unreal Engine is programming with blueprints.

The blueprints contain so-called nodes and lines, connecting parameters between them and determining the execution flow (Fig. 3). A beginner will start learning blueprints immediately after getting accustomed to the IDE.

Its visual organization allows for faster implementation, algorithm comprehension, maintaining parameter compatibility and an animated execution flow. Nodes and parameter types are also distinguished by different colors, and their names imply their function in the blueprint.

Nodes have names that describe what a node does. A few of the commonly used nodes and also the nodes that the beginner needs to learn are variable nodes, branching nodes (condition, a.k.a. if-statement), loops (for-each and for-each with break, while), spawning and destroying actors, printing strings for debugging purposes and event-related nodes.

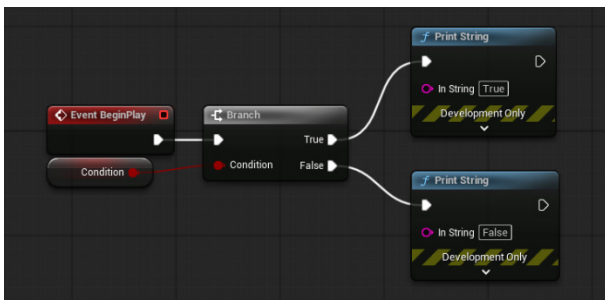


Figure 3: Blueprints

Algorithms are presented as a collection of nodes connected in a way to perform a specific action.

They allow programming without coding, eliminating or postponing learning the C++ language (the engine's primary and only programming language) until one gets comfortable with the development environment, terminology, and the language itself.

This way a beginner learns about classes such as Actor, Character, Pawn, Game Mode and so on. Each class has unique attributes and appropriate implementation and can also be extended through class inheritance.

To a beginner, the dialogue options (Fig. 4) can be confusing and overwhelming and the documentation explaining them lacks a comprehensive description.

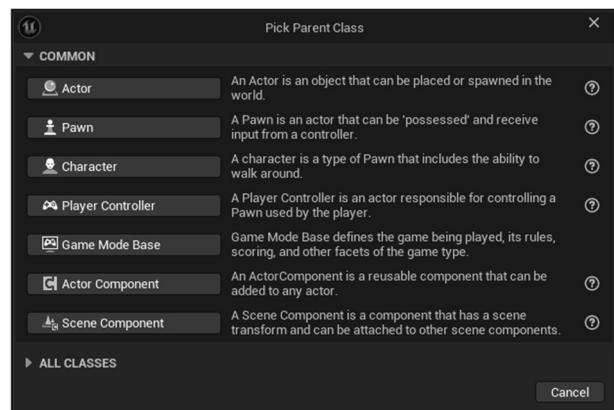


Figure 4: Inheriting options

Because of that, instead of delving into the documentation, a better approach for a young programmer would be to learn from tutorials online.

By using blueprints everyone can implement any functionality that can be programmed in C++.

However, there are some limitations to their usage, like when the complex logic implementation in a blueprint tends to become disorganized, unclear and cluttered (Fig. 5), defeating the original intention of a blueprint to be clear, readable and beginner-friendly.

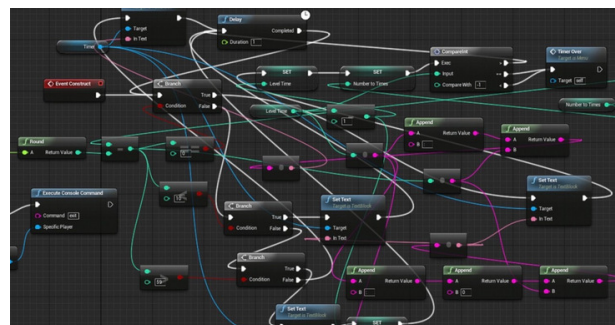


Figure 5: Blueprint limitations

3.3 Level Design

The level is a world that can be built to encapsulate the game mechanics and allow, while running the game, the player to explore it.

A good idea is to immediately make a parkour-like game (Fig. 6) since it requires only the basic knowledge of object transformation.

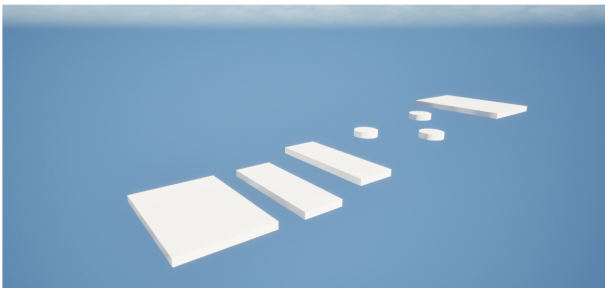


Figure 6: Simple platform game

By tweaking existing blueprints or making new ones, even a beginner can make simple improvements. This helps with motivation and self-confidence.

4 Other Unreal Engine Features

After learning the basics, it is advisable for a beginner to start developing his own game. This way he or she will be exposed to some other engine concepts in a natural way.

4.1 User Interface

The simplest feature to learn after the basics is without a doubt the engine's solution for creating a user interface, called blueprint widgets (Fig. 7).

One can write code for the widgets in a manner almost identical to the one used in normal blueprints. The only difference is the visual representation while blueprints are manipulating UI elements.

The editor supports adding different elements and configuring their properties and the changes made in a blueprint widget can

be seen in real-time in preview mode or later in a game.

Watching tutorials with UI basics is recommended first. Afterwards, if one needs an unfamiliar element, it can be searched for and placed in the UI and experimented with in the now familiar way.

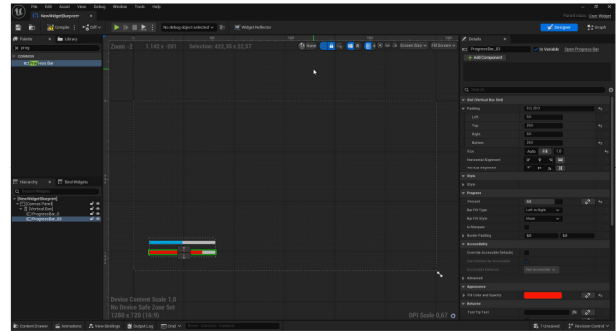


Figure 7: UI-User interface in progress

4.2 Materials and Shaders

In Unreal Engine, materials can be edited using material graphs. They are visual scripts that are later compiled to be used with shaders. Before making any material, it is good to know how textures are mapped to 3D models and how the 3D models are made.

There are many domains of materials, such as surface, decals, volume, user interface, etc. The easiest material to start with is the surface material, which can be used on 3D models.

When creating materials, the user probably slowly realizes that the mathematical knowledge he has is lacking. That is because the materials are in the end just pure mathematical functions.

For example, if one wants to make a nice shade of glow on top of a sphere, he needs to understand what a dot product between the up-vector and the vertex normal represents, which he did not even know it existed, let alone realized that it is non-commutative. The best solution to this problem is studying mathematics along the way.

One trick that also helps quite a lot when making materials is that you can imagine graphs like a compositum of functions (if one knows what a compositum is).

For example, if one wants to make a soft blend at the edge, one can use the quadratic function and shift it so that 0 is at the edge. This can be seen quite clearly when looking at the graph of that function (Fig. 8).

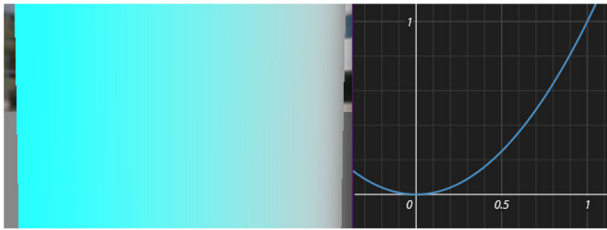


Figure 8: Visualization of function graph and its effect on the material

4.3 Other features

There are a lot more features in Unreal Engine, like animations, audio, Niagara VFX, and others. But it is not recommended to learn them as you start because they can get overwhelming and impede the learning process.

5 C++

Development of a game sooner or later reaches the point, when the performance bottlenecks start to impact the flow, framerates, loading times, etc., and it is necessary to reach for advanced tools and the C++ programming language.

However, this is quite an advanced topic in Unreal Engine and not a beginner friendly one. It is better left for the later stages of the learning process.

5.1 C++ vs Blueprints

Nevertheless, it is good to at least know one can do almost everything in both C++ and blueprints.

The problem many programmers and developers encounter, is how to decide when to use which.

If one does not have solid experience with C++, has not been planning on learning it and worked only on small projects, it is better to stick to blueprints.

However, if one worked on a bigger project and is quite familiar with C++, then it is a good idea to combine blueprints with C++ code, because it is easier and faster to write the code and maintain it later. This way, one can avoid aligning and connecting blueprint nodes, saving up quite a substantial chunk of time.

Unreal Engine ships its own C++ libraries and keeps the syntax from the C++ intact. It is not recommended to learn all the functions and classes at once, but rather as you go.

So, when one wants to make a specific feature, it is best to learn only about that of the engine. And if one does not know what is even relevant to the feature, it is probably best to just ask an AI, since it is the fastest way to get an explanation and a possible solution.

There is still that huge amount of pondering over what goes in C++ and what goes in blueprints. Probably the best approach is that most core functionality is written in C++. Blueprints are typically used to inherit from and extend C++ parent classes, allowing rapid iteration without recompiling native code. The other way is a lot harder and impractical.

For asset references, it is best to put them in the blueprints, because it is a lot easier to manage them there. Parent classes for the important features are best to be written in C++; however, the child classes are easily created and maintained as blueprints.

What to put in a parent C++ class and what in a blueprint child is the developer's choice. Some advantages of C++ are that the code is

clean, and it is easier to write complex algorithms. For blueprints, they compile very fast, so tweaking default variables and experimenting with what works is a lot faster. On the other hand, huge chunks of blueprint code can get messy very fast.

5.2 Multi-player in Unreal Engine

Before starting with multi-player in Unreal Engine, one should already know what Client-Server and Listen Server architectures are and what general networking concepts are.

Making a multi-player game in Unreal is not that different from a single-player game because Unreal handles most of the things needed by itself.

Still, a developer must keep in mind that the server application should never trust clients. All the relevant game events should be server-authorized to prevent cheating or race conditions. The potential solutions do not require that much more work.

When making a game, and when making the decision whether the game is going to be multi-player or single-player, or whether the multi-layer feature is going to be added in the latter stage of development, it is better to start the development with the multi-player feature in mind from the beginning, since developing in that way does not cause that much overhead as opposed to going the other way, when the game is already half finished.

Beginners should also familiarize themselves with basic replication patterns (e.g., RPCs, variable replication, and client-server ownership) in the first place before attempting multi-player features.

6 Making Your First Game

Unreal Engine is notorious for its steep learning curve. In order to conquer it, the best way

is to start making small games or projects and gradually ramp up their complexity. Unreal Engine already comes with some templates to start with.

For a beginner, it is best to start with game mechanics and leave assets and graphical polishing for the end. Otherwise, the sense of progression is lost and motivation is soon gone. For this reason, it is also a bad idea to try making an open world, horror or AAA game, since it is too much work for a single person. Learning Unreal Engine and making games is already enough mind-taxing and time-consuming.

6.1 Our Projects

Throughout our high school and even years before that, we accumulated some experience with Unreal Engine, C++, VR development, graphics APIs, modeling in Blender and other tasks related to game development and programming.

At the time of the publication, we are even leading learning courses for fellow students in our school. That way we learned a lot about how to present the development process and tasks to complete beginners. During this quest, we made some games on our own and got a lot of knowledge and experience that we used to disseminate in those courses.

6.2 Mystic Ascension

Mystic Ascension by Niko Maren (Fig. 9) is an Open World MMORPG (Massively Multiplayer Online Role-Playing Game) which means that there is a single shared world where all players explore, unlock and upgrade skills, wander around, admire the landscape etc.

This game is a perfect example of how not to start as a solo developer unless you intend to spend thousands of hours before seeing any usable result.



Figure 9: Mystic Ascension

6.3 Tilen's Survival Game

Trip to Mars 2 by Tilen Šimenc (Fig. 10) is the second in the series of survival games. It is an upgrade from his first game, Trip to Mars (Fig. 11), which was made when he started with Unreal Engine almost 5 years ago, when he was still attending his elementary (K-8) school.

The development started as an experiment and like other experiments of this kind, the development is still in progress.

Its goal is to survive on Mars and find a way home. The author decided to 1-up the first game because he wanted to see the progress in his knowledge.

Before this game, he also attempted to make a horror game, but after some time he realized that good horror games also need a good story, compelling environment and for an unpaid solo developer it would be very time and resource consuming.

It would require storytelling, careful planning, developing mechanics, etc., all of that being too much work for a single developer still in high school.

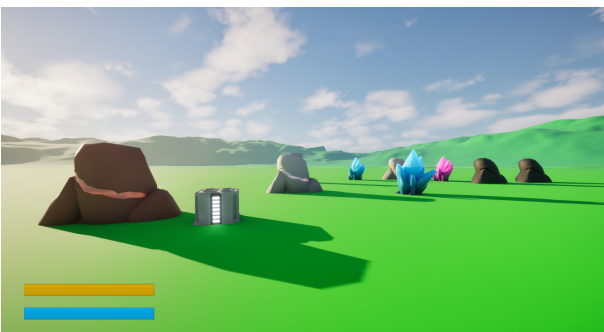


Figure 10: Trip to Mars 2

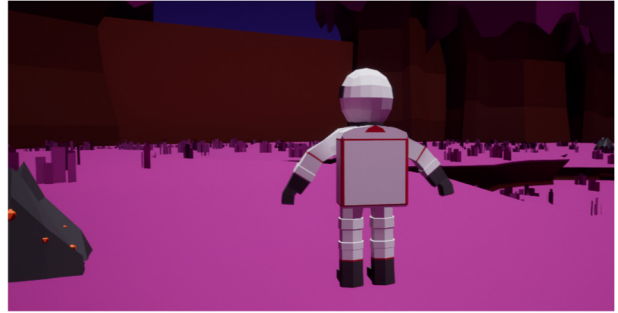


Figure 11: Trip to Mars

7 Virtual Reality

Making games for VR (Virtual Reality) in Unreal Engine is very similar to making games for PCs. The biggest difference between those platforms is designing gameplay elements and handling player input, because interactions in VR are very different from those on PCs.

Our first encounter with VR was when starting with the development of a game called BitFactory (Fig. 12). We made it as a concept sandbox game, whose purpose is to help learn the basics of computing in a fun way.

One of the many things we had trouble with was the very final step, namely making a game running on VR headsets themselves. The trouble arose mainly because of many issues in the Unreal Engine itself, limitations of the VR headsets, their graphics capabilities and performance related glitches.

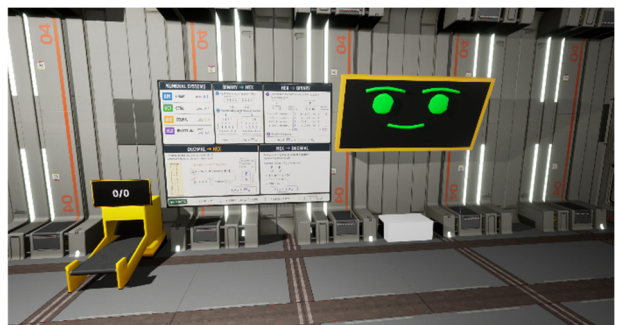


Figure 12: BitFactory

8 Conclusion

In this paper we tried to demonstrate an approach to using the Unreal Engine as self-taught developers, suggesting similar approach in education, and based on our experience.

Learning Unreal Engine requires a lot of time, an inquisitive mind and determination because of so many features the engine offers. It also has a steep learning curve, which repels beginners, since it looks unconquerable.

The second real obstacle (in this economy) is that the Unreal Editor requires at least a mid-range PC or a workstation, which is not readily available and nowadays too expensive for interested students.

Another requirement would be a strong or at least flexible mathematical background. This problem is eased quite a bit while progressing through high school. The upside here is that you immediately notice the applications of high school math problems.

Luckily for developers, when developing different types of games, such as single-player, multi-player, VR, etc., one does not need to learn everything from scratch, because the development is mostly the same no matter what type of game.

Still, based on our experience, while this approach will work well for a single developer, there is also much more to learn and adapt to, when developing in a team.

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Design and Implementation of a 6-DOF Stewart Platform Motion Simulator for Racing Applications

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Abstract: This paper presents the construction procedures of a fully functional racing simulator based on a Stewart platform with all 6 degrees of motion.

Keywords: motion simulation; Stewart platform; sim racing

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1 Introduction

Motion simulation systems enhance immersion in racing and flight simulators. The most common motion sims have 2 or 3 degrees of freedom (DOF), while more complex ones have six. Because commercial sims could carry a price of several thousands of euros, I've decided to build my own.

I decided to build a 6-DOF simulator, based on a Stewart platform with linear actuators. Because linear actuators were chosen, all the linear degrees can be expressed better.

The primary project objectives are to design and construct a mechanically-sound, stable 6-DOF Stewart platform, suitable for sustained racing, while using open-source programs.

This paper presents the tasks taken, from designing the construction and custom-made actuators, selecting components, assembly, exploring the software options, tuning the parameters, and testing.

2 Materials and Methods

Due to its size and forces involved, the setup required careful considerations regarding the geometry and forces involved. For this reason, I opted for the so-called Stewart platform and decided to design my own linear actuators.

2.1 Mechanical Design and Geometry Optimization

The Stewart platform geometry was taken from DR Sim Manager Linear Hexapod Configurator [1]. Measurements of the bottom platform were adjusted to enable easier transport of the project.

Linear actuators were custom built for this project. Main components needed to be made from aluminum and plastic. The total travel length of the actuators was designed to be 600 mm, while the usable travel is 5 mm less to prevent abruptions at the physical end-stops.



Figure 1: Finished actuators

The frame was constructed from standard 40×40 mm aluminum structural framing profiles (Bosch Rexroth [2]). Joints were reinforced with custom-made bent stainless-steel plates, cut with a laser cutter.



Figure 2: Aluminum frame

The upper moving platforms dimensions were based on calculations by the DR Sim Manager Linear Hexapod Configurator [1] and my measurements.

Platform dimensions and joint coordinates were exported from the configurator and manually scaled as needed.

Actuators were mounted to the platform using ball joints.



Figure 3: First test on a fully-assembled hexapod

Mounting brackets for all the peripherals were made with the same method as the previously mentioned reinforcements.

2.2 Component Selection

Custom linear actuators were made as replacements for commercially unavailable long-stroke (500–600 mm) electric linear actuators, which would offer high speed and fit within budget limits. Actuators are based on leadscrews and driven by ST80 alternating-current (AC) servo motors.

Each motor has 2.39 Nm of torque at 3500 rpm. If we calculate the push force of the actuators at the motor's peak power and 10 mm step of the leadscrew, we get something over 1500 N, which is enough to manipulate approx. 150 kg. This means the whole setup can be safely and fully extended while accomodating 3 occupants, and combined with the speed of the rotation, a full 600 mm travel can be achieved in a bit over a second.

For the motor control, AASD-15 dedicated servo drivers were chosen, with properties such as closed-loop position, velocity feedback, configurable acceleration and deceleration profiles, and built-in over-temperature protection (automatic throttle reduction above 60 °C, shutdown above 75 °C) [5].

The wiring is shown in the diagram below:

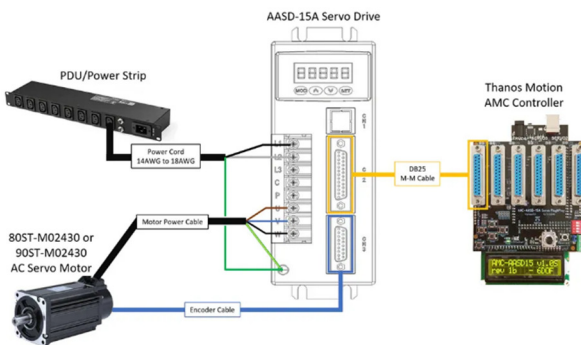


Figure 4: Wiring diagram [8]

The main controller needed to be compatible with AASD15, so Thanos AMC [3] was chosen. Buying a premade controller like this, instead of building one, was a smarter choice since it is really complex to manufacture one.

2.3 Control Architecture and Real-Time Software

The control system integrates telemetry from a racing simulator (UDP protocol via Dirt Rally 2.0 telemetry stream [7]). The easiest way to manage and filter all the parameters was to use FlyPT Mover [4]. This is an open-source motion simulator software, whose core functionality is written in C++ and features a Python configuration interface.

FlyPT mover comes with a plethora of options, configurations, filters, hardware-specific support, visualization diagrams, 3D previews and much more. The learning curve was very steep but rewarding as stacking multiple filters over each other was required to achieve a smooth motion [8].

The process of configuration took over 20 h of work and multiple accidents that broke many components.

The configuration was only done for one game, with possibilities to connect other games to the same settings. Results in behavior of the sim may vary for other games.

2.4 Testing and Validation Methodology

The aforementioned accidents made one thing very clear: the motors in the actuators are too strong for the structure.

During another accident involving caused by a programming error, the wrong actuators extended at full speed, causing the upper frame to bend.

This was a dire warning, that one wrong move could cause a disaster, despite an emergency stop button being within hand's reach.

Another accident occurred whilst playing for a prolonged amount of time, with master gain (signal amplification) set to 0.45 (normal is 0.3). During the extended use, a bolt got loose due to the huge amounts of vibrations. This caused one of the actuators to break loose and smash into the PC, connected to the rig. Luckily, the PC survived.

Finally, the program was ready and the setup was operated for approximately 50 hours, after which the entire setup was inspected for loose fasteners and similar points of failure. Finding none, it was determined the setup was ready for use.

3 Discussion and Results

Building this simulator was harder than I expected. The biggest lesson came from accidents. They were a harsh reminder that software errors become physical damage when you're dealing with hundreds of kilograms of force.

Mechanical design taught me that theoretical models do account for vibration and cyclic stresses. However, we too often choose to ignore them and cut corners.

Real-time tuning was the most tedious part. Getting a smooth motion required hours of filter configuration and tweaking the parameters.

Despite the setbacks, it works. After extensive testing, the setup performs as expected, which feels rewarding after all the failures.

The biggest lesson is that building something functional at this scale requires safety constraints and respect for the physical forces involved.



Figure 5: Finished simulator

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