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BiCMOS CIRCUIT DESIGN USING THE LATERAL PNP. A MODEL AND SOME CIRCUIT APPLICATIONS.

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ABSTRACT: This paper presents a SPICE model for the lateral PNP bipolar transistor that can be formed in a standard CMOS process with the p+ source diffusion and the n-well. This lateral PNP has an uncommitted collector, unlike the vertical PNP whose collector is always tied to the most negative supply voltage. The circuit designer is thus free to mix CMOS and Bipolar devices and to exploit their complimentary properties. Some examples of BiCMOS design are presented.

Načrtovanje BiCMOS vezij z uporabo lateralnih pnp bipolarnih transistorjev. Model in nekaj primerov uporabe

KLJUČNE BESEDE:CMOS naprave, naprave bipolarne, rezine enojne, projektiranje vezij, izdelava naprav, lastnosti komplementarne, PNP transistorji bipolarni, BiCMOS vezja, PNP lateralni, modeli vezij, SPICE program računalniški

POVZETEK: V prispevku je opisan SPICE model za lateralni PNP bipolarni transistor, ki ga lahko izdelamo v standardnem CMOS procesu, kjer sta za emiter in kolektor uporabljeni P + difuziji, n otok pa je baza. Tak lateralni PNP tranzistor ima izoliran kolektor, med tem ko je kolektor vertikalnega PNP tranzistorja vedno vezan na najbolj negativen potencial v vezju.
Načrtovalec tako lahko pri načrtovanju vezij uporabi CMOS in bipolarne komponente ter izkoristi njihove komplementarne lastnosti.
V prispevku je prikazanih nekaj primerov načrtovanja gradnikov integriranih vezij v BiCMOS tehnologiji.

Introduction.

Fig 1 shows the process cross section of a lateral pnp transistor fabricated on a standard CMOS n-well process. The transistor base width is determined by the polysilicon in exactly the same way as the MOS channel length. The majority of carriers injected into the n-well base are collected by the active collector, Ca, which completely surrounds the emitter. A minority escape into the substrate where they are collected by the substrate collector, Cs. This structure behaves like a lateral pnp and a vertical pnp in parallel, the emitters and bases being common, the collectors separate. This transistor

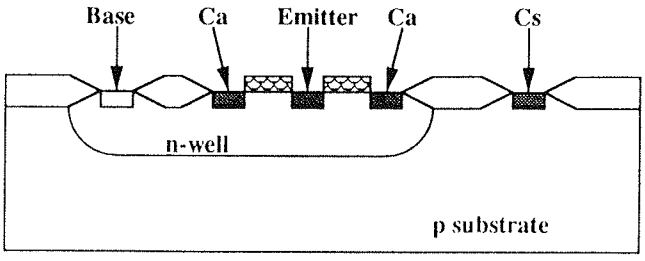

Fig. 1: Process Cross Section.

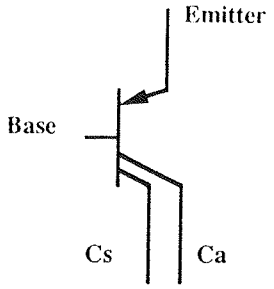

Fig. 2: Lateral PNP Symbol.

has been reported by several authors /1/, /2/. Fig 2 shows the double collector symbol for this device.

The Lateral PNP Model

Fig 3 shows the mask layout for the pnp used in the described circuits. We wish to maximise the lateral transistor action from the emitter periphery to the collector and minimise the vertical action from the bottom of the emitter down into the substrate. Therefore the emitter geometry should have the longest periphery to the smallest area. A minimum sized emitter fulfills this condition, 6 μ x 6 μ in our case. Assuming the current gains

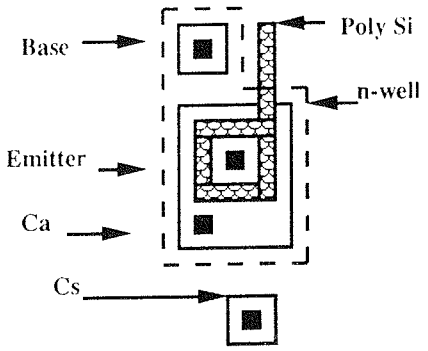

Fig. 3: Mask Layout.

are large enough to allow us to ignore base current, the emitter current, Ie, divides between the two collectors, Ca and Cs, as:

$Ica = \alpha \cdot I_e$ and $I\,cs = (1 - \alpha) \cdot I_e$

The current gains are defined as:

$$\beta_L = \left(\frac{Ica}{Ib}\right) \text{ and } \beta_V = \left(\frac{Ics}{Ib}\right)$$

Fig 4 shows a typical plot of β_L against Ica. At very low currents β_L is reduced by "weak injection effects". The

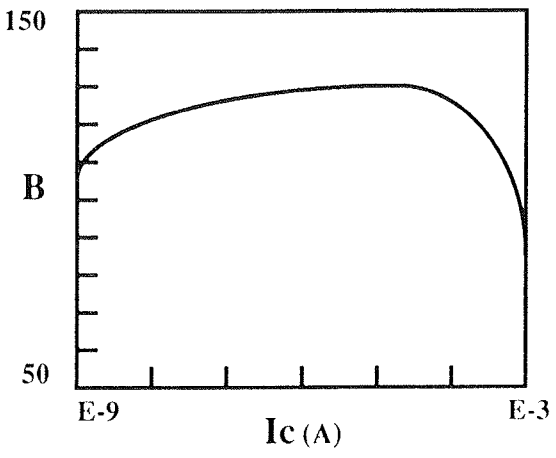

Fig. 4: B versus Ica.

principle one being that a proportion of the minority carriers injected into the base recombine at the sites of surface defects. At higher current levels "strong injection" dominates and the surface recombination is negligible. The useful current range for this device is 10^{-8} to 10^{-4} A.

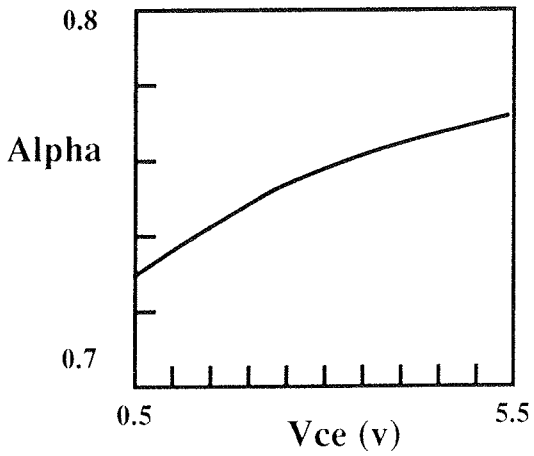

Fig. 5: Alpha versus Vce.

The division of the collector current into two parts, Ca and Cs, is very significant from a circuit design point of view. Unless the application requires both collectors to be connected to V-, the Ics current is effectively lost. So it is very important to characterise α. Fig 5 shows a typical plot of α against Vce. For this particular n-well process α varies from about 0.72 to 0.78. The model uses an average value of 0.75.

The Early voltages for the two transistors are quite different. This effect comes from the modulation of the depletion width of the base collector junction by the collector voltage. In the case of the lateral transistor this effect is severe and corresponds exactly with MOS channel length modulation. Early voltages of 10 to 15V are typical. The vertical transistor base collector junction is the n-well to substrate junction. These two lightly

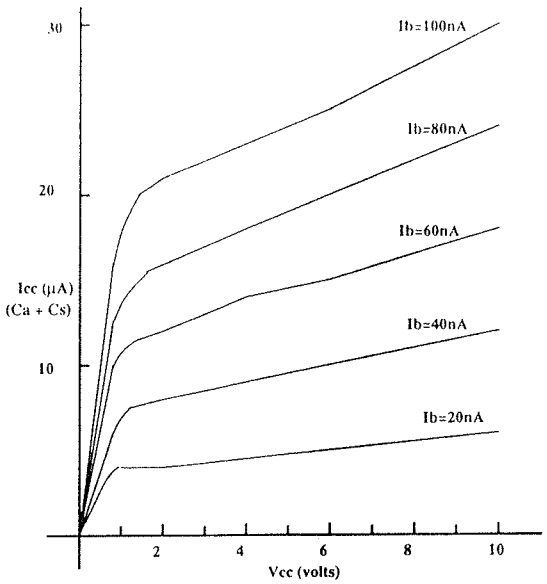

Fig. 6: Composite transistor Characteristics

doped regions have very little depletion region width variation so the vertical transistor Early voltage is very high, 100 to 300 V being typical. Fig. 6 shows typical transistor characteristics for the composite device.

The SPICE Model.

The vertical and lateral components of the transistor are formed into a SPICE code subcircuit as below:

```
.MODEL LATPNP PNP BF = 150 VAF=15 IS=2.5E-16
IKF=1 M ISE=5E- 19 NE=1.05 NF=1
.MODEL VERPNP PNP BF=9999 VAF=300 IS=9E-17
IKF=1M NF=1
.SUBCKT LPNP 100 101 102 103
**order is Ca Cs B E**
Q1 100 102 103 LATPNP
Q2 101 102 103 LATPNP
.ENDS
```

Example (1): A Band Gap voltage reference circuit.

Fig 7 shows a typical BiCMOS bandgap reference circuit fabricated in n-well CMOS technology. The bipolar pnp transistors are lateral devices as described above. The as are necessary with metal. The op-amp output is the band-gap reference voltage and can be shown to be:

$$V_{BG} = V_{be} + V_t \frac{R_1}{R_2} \ln N,\ V_t = \frac{kT}{q}$$

N = ratio of emitter areas, 6 in this case

In the proces used here the n-well sheet resistivity is 2.1K/sq. and the designer chose R1/R2 = 13. so R2 was made a 10 sq unit resistor of 21K. R1 (=273K)was made from 13 individual 21K resistors connected in series. Note that unit resistors may be connected in any series/parallel combination and so practically any ratio can be accurately designed. SPICE simulations for this circuit are shown in the table below.

Temp.(deg. C)	0	25	50	75	100
Vref (V)	1.172	1.173	1.175	1.176	1.176
+ 15% resistors	1.168	1.170	1.171	1.171	1.172
- 15% resistors	1.176	1.178	1.179	1.180	1.181

Making R2 = 12.75 x R1 = 268 K leads to slightly better results but such fine tuning should be done on the actual silicon. Remember, you cannot get 1 % results from a 5 % model !

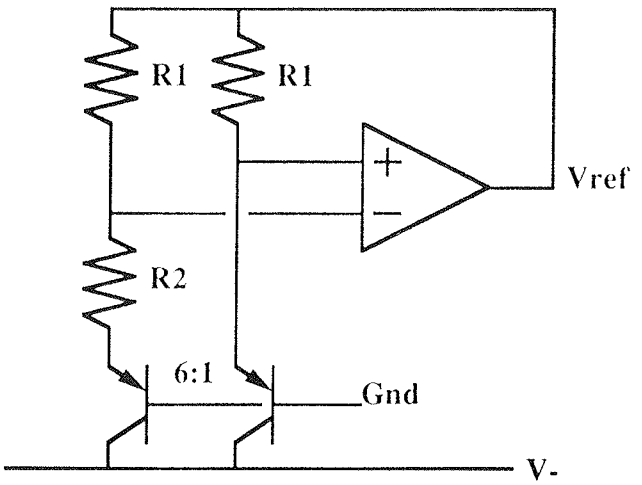

Fig. 7: The Bandgap Circuit.

CMOS Op-Amp can be quite standard. This particular circuit has the advantage that since both collectors of the composite bipolar transistor are connected to V- the current ratio between Ca and Cs is irrelevant. Precision matching of emitter areas is done with multiple copies of the same unit transistor. Precision resistor ratios are achieved by using a single unit and connecting as many

Example (2): A Differential Op-Amp Input Stage.

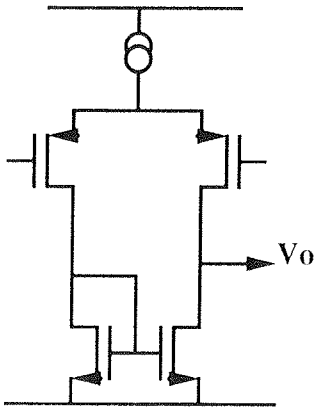

Fig. 8a: PMOS i/p devices.

Fig 8a show a standard single stage CMOS op-amp. Circuits such as this form the basic building blocks of most sampled data analog MOS circuits, frequently combined with switched capacitor techniques.

The transconductance of the MOS input transistor is given by:

$$g_m = \sqrt{2K \frac{W}{L} \cdot I_D}$$

We can replace the PMOS input transistors with PNP bipolar ones as in Fig 8b. The transconductance of the bipolar pnp transistor is now given by:

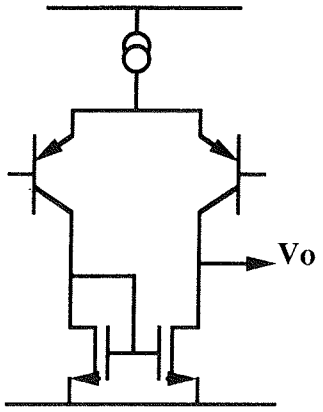

Fig. 8b: PNP Biplolar i/p devices

$$g_m = \frac{I_C}{V_t}$$

Assuming typical MOS parameters such as W/L = 10, K = 40μA/V2, we can tabulate the MOS and Bipolar gm for various bias currents.

Ic = Id	1 μa	10 μA	100 μA
MOS gm (x 10E-3)	0,028	0.09	0.28
Bipolar gm (x10E-3)	0.04	0.4	4.0

At bias currents above 1 μA the pnp bipolar input stage clearly has more gain. The table below gives some SPICE simulations for a load of 0.5pF.

Ic = Id	1 μa	10 μA	100 μA
MOS Gain (db)	45	35	25
MOS Band Width (MHz)	2.5	7	20
Bipolar Gain (db)	52	50	49
Bipolar Band Width (MHz)	4	30	200

If the supply of input base current can be tolerated then the circuit with bipolar inputs has a superior performance in every case, but particularly at higher bias currents. Such an op-amp will be used in high frequency continous time filters. The all MOS input stage is likely to remain the choice for switched capacitor speech filters.

The composite lateral pnp has a low Early voltage (reduced output impedence) so the NMOS current mirror load has been kept for both circuits.

Conclusions

Standard CMOS processing can give very useable bipolar transistors. A SPICE model for the lateral/vertical pnp bipolar transistor has been presented to enable BiCMOS circuits to be simulated and two practical design examples have been described:

(1) A Band Gap reference with 14mV variation over 0-100 deg. C and process extremes.

(2) A high performance 200 MHz op-amp with pnp input devices.

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