

# THE PIN/TCO/NIP SOLAR MODULE

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**Abstract:** Solar cells made from amorphous silicon normally have the structure pin and degrade under prolonged illumination. This paper proposes a new cell type with the structure pin/TCO/nip. Using a suitable module design, an integrated solar module can be produced with laser patterning. The incorporation of buffer layers at the n/i and i/p junctions in nip cells improves their performance, making it as good as that of pin devices under illumination through n. In initial pin/TCO/nip cells, the total efficiency is higher than in the front pin cell alone.

## Sončni modul s strukturo pin/TCO/nip

**Ključne besede:** moduli solarni, celice sončne, a-Si silicij amorfni, pin strukture pozitivno-notranje-negativno, polprevodniki, nip strukture negativno notranje-pozitivno, TCO oksid transparentni prevodni, TCO plasti, celice sončne z izkoristkom zelo visokim, celice sončne tankoplastne, silicij polikristalinični, a-Si:H silicij amorfni hidrogeniziran, SWE Staebler-Wronski efekt, pin/TCO/nip strukture paralelne, risanje vzorcev lasersko, i-plasti notranje

**Povzetek:** Sončne celice, izdelane iz amorfne silicija, imajo ponavadi strukturo pin in degradirajo, če so izpostavljene daljši osvetlitvi. V prispevku opisujemo novo sončno celico s strukturo pin/TCO/nip. Ob uporabi ustreznega načrtanega osnovnega modula lahko izdelamo integriran sončni modul s pomočjo laserske litografije. Dodane plasti na n/i in i/p spojih nip celic izboljšajo njihove lastnosti, ki postanejo primerljive s pin celicami, ko jih osvetlimo skozi n plast. V pin/TCO/nip celicah je celoten izkoristek višji kot pa pri sami pin celici.

### 1 Introduction

The research work in the field of photovoltaics for terrestrial applications comprises two basic directions: One is the development of very highly efficient solar cells made from crystalline silicon /1/ and the other is the development of thin-film solar cells. The latter direction has the advantage of reduced material consumption, which is very cost effective. Thin-film solar cells can be made from various materials, e.g. CdTe /2/, CIS /3/, polycrystalline silicon /4/, and hydrogenated amorphous silicon (a-Si:H) /5/.

The conventional a-Si:H solar cell has the structure pin. For small areas, the maximum achieved efficiency with this cell type is 13 % /6/. For larger areas, the initial efficiency of solar modules is already greater than 10 % /7/. The main application for amorphous silicon solar cells is in consumer products such as watches, pocket calculators and small battery chargers. However, the use of a-Si:H solar modules in power applications is impeded mainly by the light-induced degradation of performance during operation (Staebler-Wronski-Effect, SWE) /8/.

Several investigations have shown that the SWE is not a direct interaction between the material and the light but an indirect one. The photogenerated carriers can recombine or can be trapped in defect states within the material, and this leads to the production of metastable states. Although the microscopic origin of the effect is still not clear, it has been shown that a reduction of recombination or trapping probability will improve the stability of the cell. One way to do this is to increase the electric field across the i-layer in the pin structure. For this, thin i-layers are required /9/, but then the absorption path for light is also reduced and leads to smaller photocurrents.

Sufficient light absorption together with a strong electric field can be obtained in multi-junction solar cells /10/. These structures consist of thin single pin junctions stacked upon each other. The summation of such junctions leads to a sufficient total cell thickness. Double-junction solar cells, in which the individual junctions are made from the same material, are called double-stacked cells. The junction facing the incoming light is called the top cell while the remaining one is the bottom cell.

Conventionally, double-stacked solar cells have the structure pin/pin and are electrically in series. Although these devices behave more stably than single-junction cells [10], their main disadvantage is that the photocurrent generated in both junctions has to be equal. This represents a very stringent condition with respect to the two i-layer thicknesses. Stability requirements dictate an upper limit for the i-layer thickness of the bottom cell of approximately 350 nm, and this consequently demands very thin i-layers of less than 80 nm for the top cell. This stringent requirement is even more problematic for large area solar module fabrication because of the thickness fluctuation and the use of textured substrates. An additional restriction is that the photocurrent matching condition can only be optimized for one spectral distribution of the sunlight irradiance. Changes in the solar spectrum during the day or the year always lead to a reduction in the conversion efficiency of the total stacked device.

One can avoid these problems along with the current matching requirement by connecting the two junctions within the double-stacked configuration electrically in parallel [11]. Then, the generated photocurrents simply add up and only the photovoltages generated at the maximum power point have to be equal in both diodes. In this paper, we wish to demonstrate how a double-stacked solar module with parallel connections can be implemented and to describe the advantages as well as the problems with this type of module.

## 2 Cell design and fabrication

### 2.1 The pin/TCO/nip design

The stacked cell with parallel connections can be implemented by depositing the layer sequence TCO/pin/TCO/nip/TCO. Fig. 1 shows the basic device structure in detail. On a glass substrate coated with a transparent conductive oxide (TCO), first the pin diode is deposited with conventional deposition parameters. For the front TCO layer, for example, fluorine-doped SnO<sub>2</sub> or boron-doped ZnO can be used. After the a-Si:H pin deposition, a second TCO layer follows in order to contact the

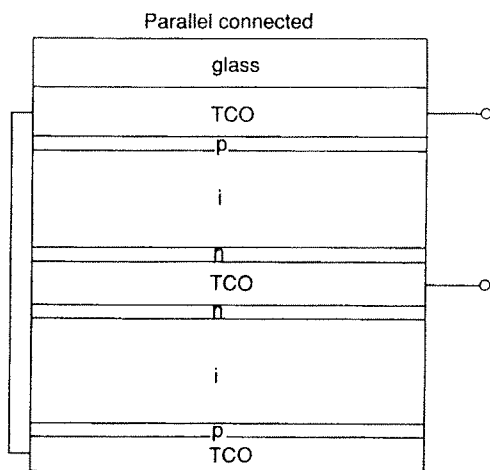


Fig. 1: Basic device structure of the parallel-connected stacked pin/TCO/nip solar cell.

n-layer. For this TCO layer, doped ZnO is a suitable material because of its low process temperature (170°C) at which no damage of the underlying a-Si:H layers occurs. The deposition of the nip diode is made with the same conditions as for the pin diode, but with the reversed deposition sequence. The third TCO layer, the back electrode, completes the device. This solar cell structure represents a three-terminal device. The parallel connection of the two subcells is made by externally connecting the front and back TCO electrodes. The implementation of the parallel connection can be made in an integrated solar module. Fig. 2 shows a cross-sectional view of such an integrated solar module. The five different patterning steps have to be performed immediately after the deposition of the layer. The front TCO is patterned into stripes by laser scribing, the lift-off technique, or mechanical patterning. For the patterning of the a-Si:H pin layer, laser scribing is best. This second cut must be offset slightly from the first one. The second TCO layer is patterned slightly beside the second cut. The patterning cuts of the a-Si:H nip diode have to lie above the cuts of the pin diode and the front TCO layer, respectively, (i.e. cut 4 is above cut 2 and cut 5 is above cut 1). With this arrangement of the patterning cuts of the two diodes (subcells) and the three TCO layers, two connecting modes are implemented. The parallel connection is implemented by connecting the two p-layers of one solar cell stripe. The series connection is made by connecting the n-layer (middle TCO-electrode) of one solar cell stripe with the p-contact (front and back TCO-electrode) of the neighboring solar cell stripe. For clarification, a circuit diagram is also shown at the top of Fig. 2.

The modelling of the light characteristics of a parallel connected stacked solar cell was performed with a simulation program using numerical methods to solve the Poisson equation and the continuity equations for electrons and holes [12]. Fig. 3 shows simulated current-voltage characteristics and AM1.5 sunlight of the total stacked device together with the characteristics of the two subcells. The thicknesses of the two i-layers were 200 nm and 400 nm for the top and bottom cell, respectively. As can be clearly seen, the filtered light

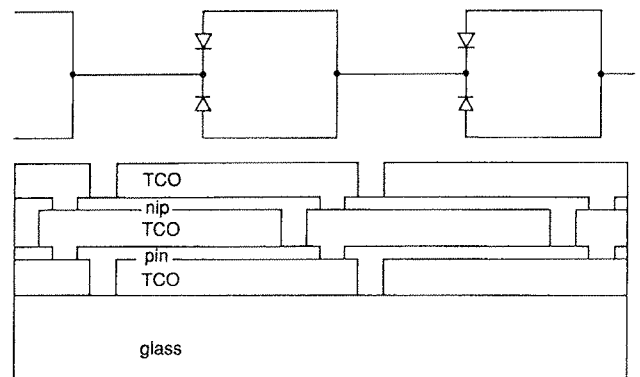


Fig. 2: Cross-sectional view of the integrated solar module, consisting of parallel-connected stacked solar cells together with the related circuit diagram.

from the top cell only generates a small short-circuit current in the bottom cell. However, there is nearly no difference in the photovoltage of two subcells at the maximum power point. Therefore, the output power of the individual subcells adds up with almost no electrical loss to the output power of the total device.

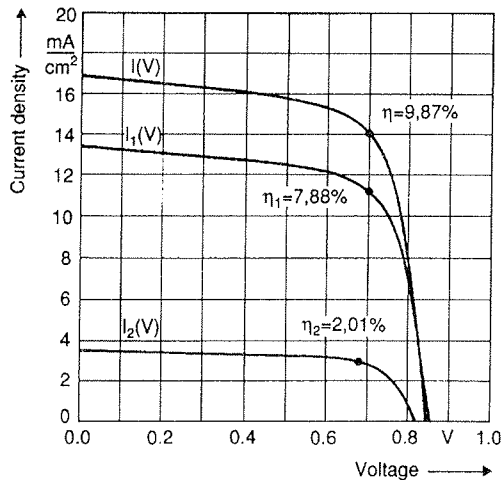


Fig. 3: Computed current-voltage characteristics under AM1.5 light of the individual pin and nip cells in a stacked solar cell and of the composite pin/TCO/nip parallel connected structure

### 2.2 Amorphous Silicon Technology

For the fabrication of a-Si:H films for solar cells, even on an industrial scale, the plasma enhanced chemical vapour deposition technique (PECVD) is always used /13/. Fig. 4 shows schematically a deposition apparatus. Two electrodes are located within a distance of approximately 40 mm in a vacuum chamber. Both electrodes can be heated. The bottom electrode is grounded and serves as a substrate holder. The top electrode is connected to the rf power supply and normally operates at a frequency of 13.56 MHz. The pumping system controls the pressure during the deposition process in a range from 0.1 mbar to 0.5 mbar. The gas mixing system regulates the amount and composition of the process gases used. For the deposition of intrinsic a-Si:H films, only silane gas (SiH<sub>4</sub>) is necessary. The rf transmitter burns a glow discharge between the two electrodes. The gas molecules form a plasma, are decomposed, and are partially deposited onto the substrate. By adding doping gases such as diborane (B<sub>2</sub>H<sub>6</sub>) or phosphine (PH<sub>3</sub>), one can also deposit p- or n-doped layers, respectively. Furthermore, the optical band gap can be enhanced by adding methane gas (CH<sub>4</sub>), and reduced by adding germane gas (GeH<sub>4</sub>). Etching gases such as CF<sub>4</sub> or SF<sub>6</sub> are able to clean the deposition chamber /14/. This is important for large systems that have to be cleaned regularly.

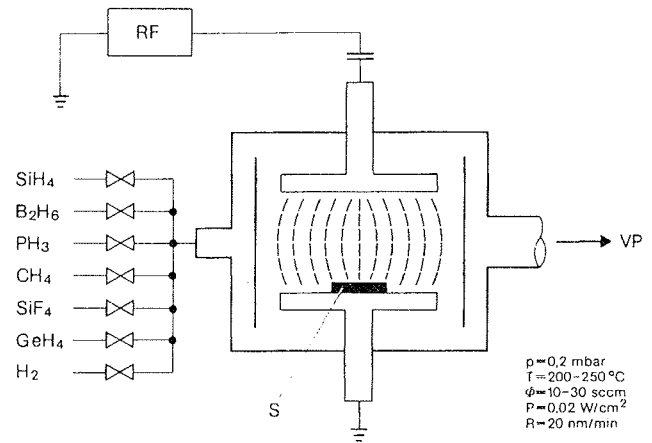


Fig. 4: Schematic view of an a-Si:H deposition system.

The pin solar cells produced in our research laboratory at Siemens AG were deposited in a two-chamber in-line system. It consists of a load-lock chamber and two process chambers. Chamber one is used for depositing the doped p- and n-layers, and chamber two is used for fabricating intrinsic material only. The chambers are separated by valves through which the substrate holder can be moved. This apparatus is able to deposit substrates having a size of up to 40x40 cm<sup>2</sup>. We used this machine to develop 10x10cm<sup>2</sup> solar modules having the structure pin or nip. The deposition conditions are described elsewhere /15/.

### 2.3 Patterning

The scribing of the cut lines in the different layers was made by laser patterning. We used two types of laser. One IR laser (1042 nm) for patterning the front TCO layer and a frequency-doubled Nd:YLF laser (523 nm) for all other patterning steps. The setup for the laser scribing is shown in Fig. 5. The two lasers are positioned at pos1 and pos2. With two surface mirrors and one lens (f = 100mm) the laser beam was focused and directed onto the sample, which was mounted on a moving table. The laser light always entered the sample through the glass substrate. For the P#1 the IR light was absorbed

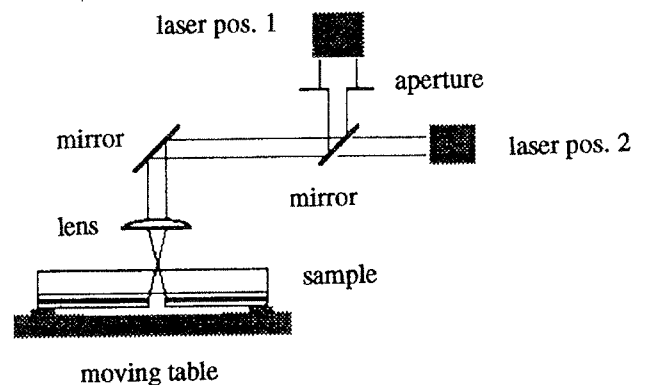


Fig.5: Schematic view of the setup for the laser patterning

in the TCO1 layer and removed the material. In all other patterning steps, the light is absorbed in the first a-Si:H layers (pin diode). The absorption leads to a considerable warming of the a-Si:H material and induces thermal expansion. As a consequence the material peels off. The effect is so pronounced that all layers deposited onto the first a-Si:H layers will be removed as well. Thus, the patterning steps P#4 to P#5 can be performed with the same technique. The details of the laser scribing are given in table 1.

Table 1: Parameter of the laser scribing

Parameter		P#1	P#4 to P#5
laser		Laser Appl. Model 9560 QT	ADLAS 321
wavelength	[nm]	1042	523
power	[mW]	800	8
pulse width	[ns]	80	15
frequency	[kHz]	4	1
focal diameter	[ $\mu\text{m}$ ]	50	50
scribing velocity	[m/min]	6	2.9

The laser scribing through the substrate required a slightly different arrangement of the patterning lines. Fig. 6 shows a schematic cross-sectional view of the patterning, again together with the circuit diagram. The distance between the P#2 and P#3 line was increased and the P#4 and P#5 lines are located between them.

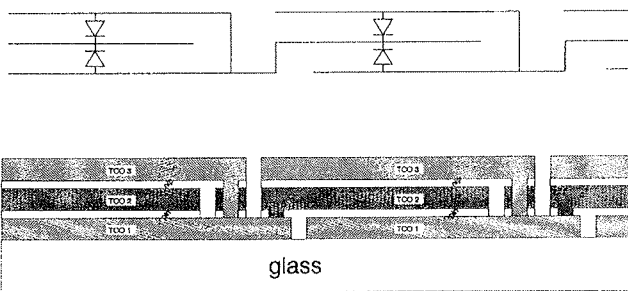


Fig. 6: Cross-sectional view of the patterning lines together with the circuit diagram

In order to control the laser scribing, REM pictures of the cross-sectional view were made. Fig. 7 shows the P#1 cut. One can clearly see that the patterning works very well. The front TCO1 is completely removed and the subsequently deposited layers show excellent covering of the P#1 line. The most critical patterning step is the P#3 line. This cut has to separate the center TCO2 layer. Furthermore, the following a-Si:H layers have to cover this cut such that no connection is made to the back TCO3 layer. Fig. 8 demonstrates that the demands

are completely fulfilled. The center TCO2 layer is removed and the nip structures cover the scribed area completely.

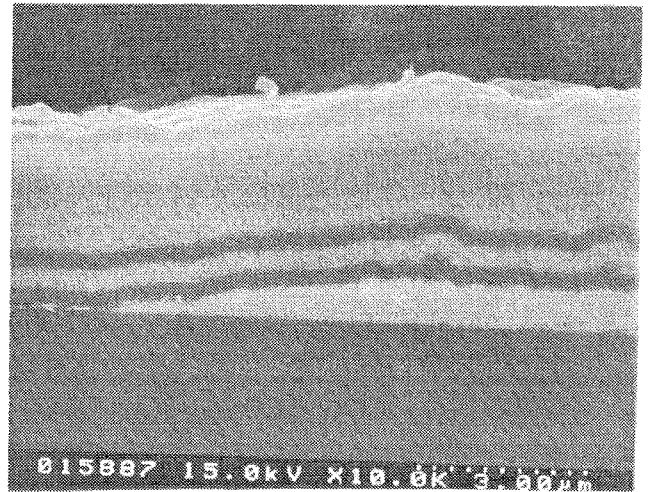


Fig. 7: REM picture of a cross-section of the P#1 line

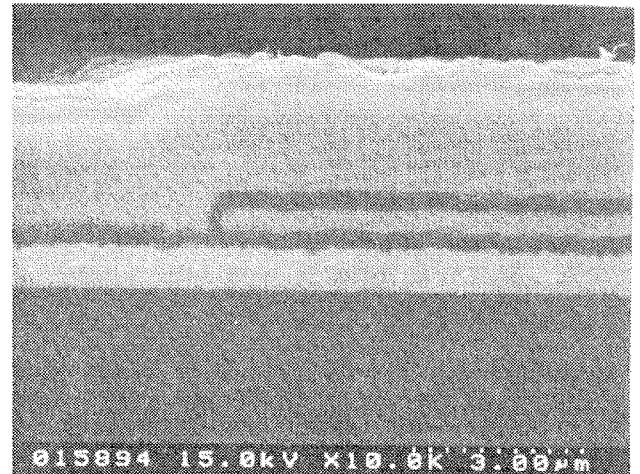


Fig. 8: REM picture of a cross-section of the P#3 line.

### 3 Results of cells and modules

#### 3.1 PIN and NIP cells

The nip structure on glass/TCO substrates incorporates two difficulties: one is the inversed deposition sequence and the second is the illumination through the n-layer. In order to distinguish these two effects, we deposited pin as well as nip diodes with p-SiC layer having transparent electrodes on both sides. The cells were then investigated by dark and light characteristics and their spectral response for illumination through both sides.

Looking first to the pin device, we summarize the results in table 2. As one can clearly see, the n-side illumination reduces all parameters of the light characteristics. In fig.

9 the short-circuit spectral response of the pin cell is shown for both illumination directions. It demonstrates that the reduced short-circuit current for the n-side illumination is caused by a poorer blue response. The possible reasons for this are that the n-layer is too thick, that the surface recombination velocity at the n/i junction is very strong, and that the lifetime of holes is not sufficient to pass the i-layer completely. The fill factor and especially the open-circuit voltage are also lower for the n-side illumination mode. The low  $U_{oc}$  value indicates a strong surface recombination velocity at the n/i and also i/p junction.

Table 2: Measured results for a pin solar cell illuminated through the p- and n-side

Parameter		p-illum.	n-illum.
$\eta$	[%]	8.44	5.96
$U_{oc}$	[mV]	840	811
$I_{sc}$	[mA/cm <sup>2</sup> ]	14.17	11.71
FF	[%]	70.9	62.8
n		1.59	1.59
$I_0$	[A/cm <sup>2</sup> ]	$1.21 \cdot 10^{-11}$	$1.21 \cdot 10^{-11}$
Q(400nm)	[%]	62.8	36.6
Q(600nm)	[%]	87.3	81.4

Table 3: Measured results for a nip solar cell illuminated through the p- and n-side

Parameter		p-illum.	n-illum.
$\eta$	[%]	5.65	3.91
$U_{oc}$	[mV]	785	746
$I_{sc}$	[mA/cm <sup>2</sup> ]	11.72	9.31
FF	[%]	63.6	56.3
n		1.48	1.48
$I_0$	[A/cm <sup>2</sup> ]	$6.46 \cdot 10^{-12}$	$6.46 \cdot 10^{-12}$
Q(400nm)	[%]	51.1	19.5
Q(600nm)	[%]	76.7	72.0

The same qualitative results are obtained with the nip diode. Table 3 summarizes the parameters. As before, p-side illumination leads to higher efficiencies than n-side illumination. But the absolute values are lower compared to the pin device. In particular, the open-circuit voltage is very poor for both illumination modes. The same holds true for the spectral response, as can be seen by comparing fig. 10 with fig. 9. The deposition

in the two chamber reactor makes it possible to achieve identical i-layer properties in both types of diodes. We thus concluded that the differences in the pin and nip diodes are primarily related to different properties of the p/i and i/n junctions.

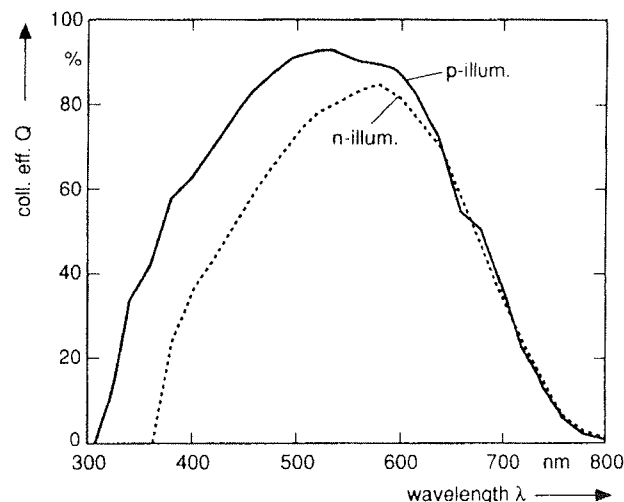


Fig. 9: External collection efficiency Q versus wavelength  $\lambda$  of a pin solar cell for illumination through the p- and n-side

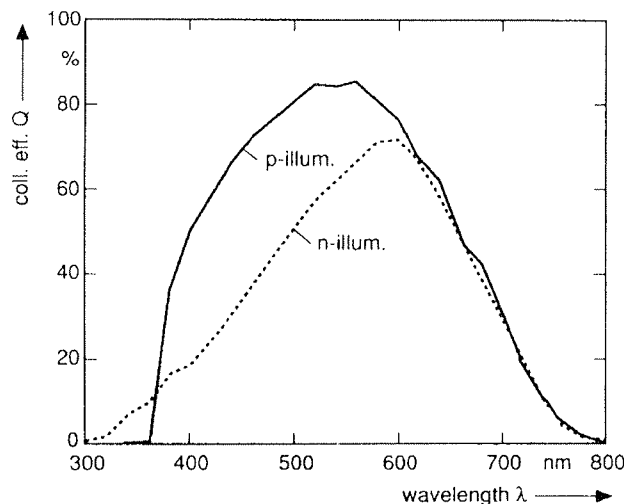


Fig. 10: External collection efficiency Q versus wavelength  $\lambda$  of a nip solar cell for illumination through the p- and n-side

### 3.2 Improvement of the nip solar cell

Several changes were made in order to overcome the above-mentioned problems. First of all, the n-layer thickness was reduced. This increased the external collection efficiency for blue light ( $\lambda = 400$  nm) to values up to 58 % and the short-circuit current to up to 11.5 mA/cm<sup>2</sup>. The AM1 efficiency was then more than 5 % being close to the efficiency value of the pin device illuminated through the n-side.

Table 4: Results of nip diodes having differently doped i-layers.

B <sub>2</sub> H <sub>6</sub> /SiH <sub>4</sub>	[ppm]	0	1.25	2	2.5	3.25
$\eta$	[%]	2.50	5.37	4.99	5.51	5.13
U <sub>oc</sub>	[mV]	735	843	869	854	930
I <sub>sc</sub>	[mA/cm <sup>2</sup> ]	6.28	10.26	10.34	10.76	10.41
FF	[%]	54.1	62.1	55.6	59.9	53.0
n		1.38	1.67	1.82	1.86	1.84
I <sub>0</sub>	[A/cm <sup>2</sup> ]	2.14*10 <sup>-12</sup>	6.90*10 <sup>-12</sup>	1.54*10 <sup>-11</sup>	3.02*10 <sup>-11</sup>	1.67*10 <sup>-11</sup>
Q(400nm)	[%]	9.3	33.8	41.1	37.7	41.8
Q(600nm)	[%]	49.5	62.4	59.7	68.6	61.1

In a second step, we tried to improve the hole properties by slightly doping the *intrinsic* layer. The doping concentration was varied between 0 and 3.25 ppm B<sub>2</sub>H<sub>6</sub>/SiH<sub>4</sub>. The results are presented in table 4. With increasing doping, the open-circuit voltage increases from 735 mV (without doping) to 930 mV (3.25 ppm). However, too much doping causes the fill factor to decrease.

Finally, the incorporation of buffer layers at the n/i and i/p junctions was also tested. Different buffer layers were used at the two junctions. Between the n- and i-layers, a boron doped buffer layer was incorporated, whereas on the other side an intrinsic a-SiC layer was used. The results are summarized in table 5. One can clearly see that the buffer layer at the n/i junction slightly improves the open-circuit voltage up to a value of 791 mV. But the major effect is an improvement of the fill factor (up to 63%). The carbonized buffer layer at the i/p junction has the greatest influence on the open-circuit voltage. The incorporation of this layer increases U<sub>oc</sub> to 844 mV, which is equivalent to the U<sub>oc</sub> values of pin solar cells. The efficiency of this cell is comparable to the efficiency of pin cells under n-side illumination.

Table 5: Results of nip diodes with buffer layers.

buffer		no buffer	at n/i	at n/i and i/p
$\eta$	[%]	2.50	5.34	5.96
U <sub>oc</sub>	[mV]	735	791	844
I <sub>sc</sub>	[mA/cm <sup>2</sup> ]	6.28	10.72	11.23
FF	[%]	54.1	63.0	62.9
n		1.38	1.36	1.60
I <sub>0</sub>	[A/cm <sup>2</sup> ]	2.14*10 <sup>-12</sup>	2.53*10 <sup>-11</sup>	6.0*10 <sup>-12</sup>
Q(400)	[%]	9.3	45.5	40.1
Q(600)	[%]	49.5	63.0	63.2

### 3.3 The pin/TCO/nip cell

The first pin/TCO/nip cells were produced using the standard deposition parameters for the pin and the improved process for nip cells. For this, we start with a relatively thick pin diode having a thickness of approximately 420 nm in order to overcome shunting problems. The thickness of the nip diode was about 500 nm. The TCO2 thickness was chosen to be as low as possible so that covering of the P#3 cut with the nip structure is effective. As a result, the thin TCO2 layer formed a relatively high series resistance and the inhomogeneity hindered the function of a complete module. In order to investigate individual pin/TCO/nip cells of a module, we made an additional patterning line as shown in fig. 11. This P#6 cut makes it possible to measure the pin, the nip and the pin/nip cells separately, because load 1 contacts the middle TCO layer. Thus, connecting the loads 1 and 3 measures the pin cell, loads 1 and 2 the nip cell, and loads 2 and 3 measures the complete pin/nip device.

Table 6: Results of the pin/TCO/nip cell and the individual pin and nip cells

cell	$\eta$	U <sub>oc</sub>	I <sub>sc</sub>	FF	U <sub>mpp</sub>
	[%]	[mV]	[mA/cm <sup>2</sup> ]	[%]	[mV]
pin	7.00	870	11.91	67.6	667
nip	0.83	698	2.41	49.3	470
pin/nip	7.24	832	14.31	61.5	616

The results of the light characteristics are presented in table 6 and fig. 12 shows the characteristics. One can see that the overall efficiency is better than the efficiency of the pin cell itself. However, the nip cell contributes little to the total efficiency because the thickness of the pin cell was too great. In order to improve the nip cell's component and the stability of the total device, the thickness of the pin front cell must be reduced.

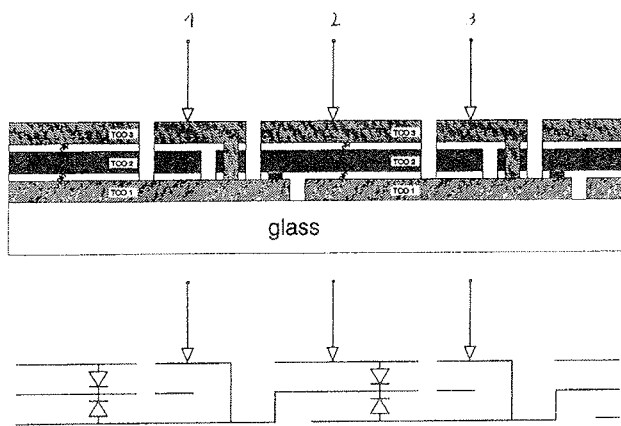


Fig. 11: Schematic view of the patterning lines for measuring the pin, nip, and pin/nip cells separately.

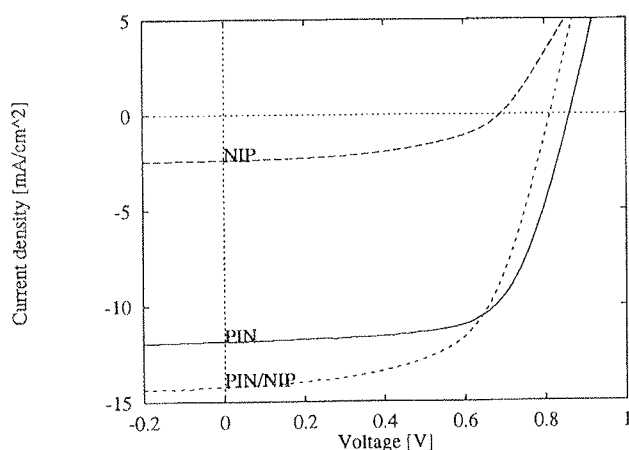


Fig. 12: Light characteristics of a pin, nip and pin/nip cell.

#### 4 Conclusion

The parallel-connected stacked solar cell represents a design for a-Si:H solar cells which meets the demands for strong electric fields within the i-layer and sufficient light absorption without the disadvantage of the current matching requirement. It has been shown that the design could work. The patterning can be done with laser scribing and nip cells can be made as efficiently as pin devices illuminated through the n-layer. However, it seems that the structure could not be deposited on textured substrates, because of shunting problems with thin pin modules. The use of smooth substrates can overcome this problem. In any case, the parallel connection is a powerful alternative to the conventional series connected stack cells.

#### References

- /1/ J. Zhao, A. Wang, P. Altermatt, M.A. Green, Appl. Phys. Lett. Voll. 66 No. 26 (1995) 3636
- /2/ T.L. Chu, S.S. Chu, J. Britt, G. Chen, C. Ferekides, N. Schultz, C. Wang, C.Q. Wu, H.S. Ullal, Proc. of the 11<sup>th</sup> E.C. Photov. Solar Energy Conf. (1992) 988
- /3/ L. Stolt, J. Hedström, M. Bodegard, J. Kessler, K.O. Velthaus, M. Rickh, H.-W. Schock, Proc. of the 11<sup>th</sup> E.C. Photov. Solar Energy Conf. (1992) 120
- /4/ J.H. Werner, R. Bergmann, R. Brendel, in Festkörperprobleme/Advances in Solid State Physics, Vol. 34 (1994) 115
- /5/ K. Takahashi, M. Konagai, "Amorphous Silicon Solar Cells" (1983) ISBN 0-946536-35-X
- /6/ K. Miyachi, N. Ishiguro, T. Miyashita, N. Yanagawa, H. Tanaka, M. Koyama, Y. Ashida, N. Fukuda, Proc. of the 11<sup>th</sup> E.C. Photov. Solar Energy Conf. (1992) 88
- /7/ W. Kusian, K.-D. Ufert, H. Pfeleiderer, Solid State Phenomena Vols. 44-46 (1995) 823
- /8/ D.L. Staebler, C.R. Wronski, Appl. Phys. Lett., Vol. 31, No. 4 (1977) 292
- /9/ P. Lechner, H. Rübél, N. Kniffler, Proc. of the 10<sup>th</sup> E.C. Photov. Solar Energy Conf. (1991) 354
- /10/ Y. Ichikawa, T. Ihara, S. Saito, H. Ota, S. Fujikake, H. Sakai, Proc. of the 11<sup>th</sup> E.C. Photov. Solar Energy Conf. (1992) 203
- /11/ J. Furlan, Proc. of the 6<sup>th</sup> Photovoltaic Science and Eng. Conf. PVSEC-6 (1992) 287
- /12/ F. Smole, J. Furlan, J. Appl. Phys. 72 (1992) 5964
- /13/ W. Krühler, Appl. Phys. A53 (1991) 54
- /14/ H. Kausche, M. Möller, R. Plättner, Proc. of the 5<sup>th</sup> EC Photovoltaik Solar Energy Conf. (1983) 707
- /15/ J.G. Grabmaier, M. Möller, R.D. Plättner, W. Krühler, Siemens Forsch. Entw. Ber. Bd. 13 (1984) 289

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