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CURRENT TRENDS IN EMBEDDED SYSTEM TEST

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Abstract: *Increasing complexity of electronic components and systems makes testing a challenging task. With the introduction of surface mounted devices, traditional in-circuit test techniques utilizing a bed-of-nails to make contact to each individual lead on a printed circuit board are becoming very costly and also inefficient. The need of an alternative test access fostered the development of novel test solutions like the IEEE 1149.1 boundary-scan architecture, recently extended to the mixed-signal test area by the IEEE 1149.4 Standard. At the chip level, technology advances allow to integrate functions that have been traditionally implemented on one or more complex printed circuit boards into one single integrated circuit. The development of such a System-on-Chip (SoC) is based on the design technique which integrates large reusable blocks (i.e., cores) that have been designed and verified in earlier applications in practice. This design technique introduces new extremely difficult test problems due to the fact that the core user (SoC designer) in most cases does not have detailed knowledge about the core design. Further difficulties represent the problem of test access of deeply embedded cores and portability of tests between core providers, SoC designers, as well as final SoC users. Embedded system testing faces all the above problems hence it is imperative to be aware of the novel test techniques and current trends in test standardization. The paper briefly summarizes current state-of-the-art and gives pointers for further research in this topic.*

Sodobni pristopi k preizkušanju vgrajenih sistemov

Izvleček: *Zaradi naraščajoče kompleksnosti elektronskih komponent in sistemov postaja njihovo preizkušanje vedno večji problem. S površinsko montažo komponent postajajo tradicionalne metode preizkušanja osnovane na direktnem dostopu posameznih točk na tiskanini preko vzmetnih kontaktov drage in neučinkovite. Potreba po drugačni izvedbi dostopa do internih točk preizkušanca je vzpodbudila razvoj novih preizkusnih metod, kot je na primer IEEE 1149.1 (robna preizkusna linija) in njena razširitev na področje preizkušanja mešanih analogno-digitalnih vezij IEEE 1149.4. Tehnološki razvoj omogoča integracijo funkcij, ki so bile v preteklosti izvedene na enem ali več v modulih sistema, v enem samem integriranem vezju. Razvoj takšnega "sistema-v-čipu" (angl. System-on-Chip, SoC) je osnovan na načrtovalskih pristopih, ki omogočajo integracijo velikih že uporabljenih in v praksi preizkušenih logičnih blokov (jeder). Ta pristop pa hkrati prinaša tudi nove, izredno težke probleme pri preizkušanju načrtovanega produkta, saj razvijalec običajno ne pozna do podrobnosti zgradbe uporabljenih jeder. Nadaljnje težave predstavlja dostop globoko vgnezdenih jeder ter prenosljivost preizkusnih postopkov med dobavitelji jeder, načrtovalci sistemov-v-čipu in končnimi uporabniki. Preizkušanje vgrajenih sistemov se srečuje z vsemi navedenimi problemi, zato je pomembno, da so razvijalci seznanjeni s sodobnimi preizkusnimi metodami in njihovo standardizacijo. V članku na kratko povzemamo sedanje stanje in podajamo glavne smernice za nadaljnje poizvedbe na tem področju.*

1. Introduction

Advances in deep submicron technology are increasing the operating frequency and complexity of VLSI circuits which makes the testing problem more and more difficult. Complex Systems-on-Chip (SoCs) with the working frequency already in excess of 1 GHz require sophisticated testers with comparable clock rate. High-speed clocks employed in today's design require at-speed test to address potential performance-related problems. Current test systems are limited in signal generation and data capture speed to about 1.6 GHz and the cost of a tester capable of applying test vectors at the above clock rate approaches $10k per pin, not to count the additional cost of signal generators and measurement instruments needed for testing mixed-signal circuits. According to the SIA roadmap /1/, the prices of ATE (automatic test equipment) system are expected to continue toward > $20 million and may reach $50 million by 2010.

Another feature that impacts on test complexity is increasing transistor density of a chip which doubles every 18 to 24 months. This trend, known also as Moore's Law, continues to hold from the mid-1970s. Testing difficulty increases due to the fact that the number of transistors in a chip increases faster than the pin count. Consequently, internal chip modules become increasingly difficult to access. As described in /2/, the increase of test complexity can be expressed by the ratio N_t / N_p, where N_t denotes the number of transistors and N_p the number of input/output pins. The two parameters are related by the expression $N_p = K\sqrt{N_t}$, where K is a constant. This relation is known as Rent's rule. Since modern technologies allow drastic increase of transistor density in comparison with the number of pins, ATE systems have to access a larger number of complex logic blocks on a chip through a proportionally smaller number of input/output pins.

Due to the costly ATE systems, currently many factories around the word have installed test capability only at about 100 MHz clock rate which no longer fulfils the requirements of at-speed test of current circuit designs. Furthermore, the growing bandwidth gap as a result of the limited number

of input/output pins prolongs the test time resulting in increased test cost.

Presented problems fostered development of new design-for-test (DFT) techniques with the goal of providing cost-effective high-quality at-speed test. In order to avoid the communication bottleneck between the high-performance ATE and the device-under-test (DUT), the *embedded test* approach /3/ implements ATE functions like high-speed generation of test vectors and response analysis together with some additional test control logic in the target DUT. In this approach, at-speed test actions are performed by the embedded test logic including pattern generation, test result compression and timing-generation. The remaining low-speed operations required for the execution of the complete test of the DUT are left to a low-cost external ATE, as shown in Figure 1. Alternatively, they can be completely integrated in the DUT in a built-in self-test (BIST) structure /4/.

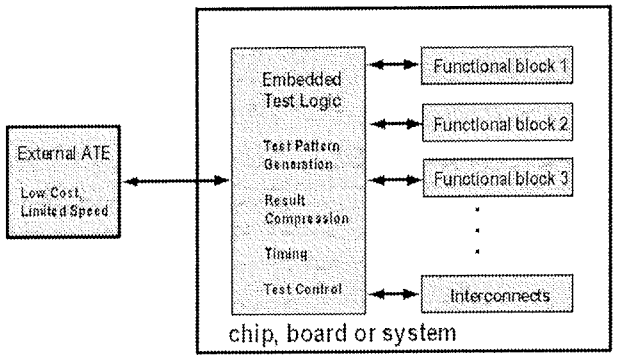

Figure 1: Embedded test configuration

Very high scale of integration of ICs introduces test problems also at other levels. Nowadays, both printed circuit board test and system test deal with very complex ICs which are by default difficult to stimulate. In addition, printed circuit boards are increasingly difficult to test by the conventional in-circuit test systems. Surface mounted devices placed on both sides of a board and smaller pin-to-pin spacing limit the access to the test points on the board, which makes the implementation of the bed-of-nails fixtures difficult and costly. The need for an alternative access of internal test points gave the idea of building the test probes directly into the chips and to connect the probes with the external ATE by simple serial line. The effort of ATE manufacturers and EDA tool suppliers organized as the Joint Test Action Group (JTAG) resulted in a *boundary-scan* test technique for digital circuits and systems and was approved as the IEEE Standard 1149.1 in 1990 /5/. The main objective was to provide standardized approaches to board interconnect test and internal test of the devices placed on it. As the standard gained popularity in practice, many other applications in test as well as in other areas have been reported. In 1999, IEEE Standard 1149.4 (Standard for a Mixed-Signal Test Bus) /6/ has been approved. This standard can be regarded as the extension of the IEEE Standard 1149.1 to the area of mixed-signal device test.

Let us finally mention the emerging IEEE P1500 Standard for Embedded Core Test /7/ which offers standardized DFT solutions for SoCs but will affect also board and system test once the chips complying to the IEEE Standard P1500 appear in practice.

2. DFT Standards

Many embedded test solutions in practice rely on the test infrastructure imposed by the above-mentioned standards. Standard test port features defined by these standards provide standard way to deliver test data to the DUT and capture test results. They also facilitate built-in self-test (BIST) implementation and provide effective means to reuse BIST and embedded test solutions at the board and system level test. For this reason we shall in the following briefly review the main features of IEEE Standards 1149.1, 1149.4 and P1500.

2.1 Boundary Scan Standard

The basic idea of the boundary-scan approach is to replace external probe or bed-of-nails pins by internal probes placed on a chip between device pins and IC core logic. During normal operation, the internal probes (i.e., scan modules) are transparent while in the test mode additional test logic is activated between the external pin and IC core in order to perform the selected test. Scan modules are serially interconnected and form a boundary-scan register around the chip. The boundary-scan register allows the application of test vectors to the IC's pins or core circuit as well as sampling of internal and external values at IC pins. Test vectors/responses are serially shifted in and out of the boundary-scan register through the device's test ac-

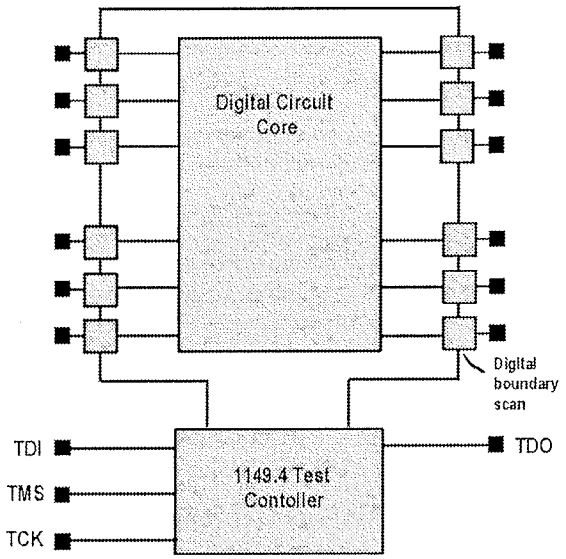

Figure 2: A schematic of a chip complying to IEEE Standard 1149.1

cess port (TAP). TAP consists of four mandatory connections: Test Clock input (TCK), Test Mode Select input (TMS), Test Data Input (TDI) and Test Data Output (TDO) and optional Test Reset input. A schematic of a chip with included IEEE Standard 1149.1 test infrastructure is shown in Figure 2. In a typical application, chips on a board are configured into one or more boundary-scan chains with common TCK and TMS connected to the external test system.

A chip compliant with IEEE Standard 1149.1 includes TAP, TAP controller and at least the following three test data registers: Boundary-Scan Register, Instruction Register and Bypass Register. TAP Controller generates control signals required for the operation of the Instruction Register and the Test Data Registers. IEEE Standard 1149.1 prescribes three mandatory instructions: Sample/Preload, Bypass and Extest. The Sample/Preload instruction is used to obtain a snapshot of the device input and output signals during the normal operation. Its execution does not interfere with circuit's normal operation, hence this option may be very useful for system debugging. The purpose of the Bypass instruction is to shorten the scan path through the boundary-scan architecture when scan access of the test data registers is not required. The Extest instruction allows test of board interconnections (i.e., test of opens, shorts or bridging faults). It can be also used to test non-boundary-scannable parts of the system. A chip compliant with IEEE Standard 1149.1 may optionally include other types of test data registers to perform non-mandatory instructions like, for example, Runbist (which runs a built-in self-test of a circuit), Idcode (which allows reading of the circuit's identification code and thus permits blind interrogation of the assembled components on a board), Intest (which allows slow speed testing of the core of a circuit), and many others.

Conventional boundary-scan tests run at the test clock TCK generated by a low cost external test system. Such configuration is primarily used for static interconnect test. However, as we shall see in the next section, one of the reported embedded test solutions extends boundary-scan test infrastructure to perform at-speed test.

2.2 Mixed-Signal Test Bus Standard

IEEE Standard 1149.4 defines the way to access the mixed-signal chips on a board in order to perform interconnect test and parametric test of discrete components connected to the chips. IEEE Standard 1149.4 provides facilities that allow to detect opens in the interconnections between chips, and to detect and localize bridging faults. The defined test infrastructure allows interconnect testing in full compatibility with IEEE Standard 1149.1. It also allows measurements of the values of discrete components such as pull-up resistors, filter capacitors, etc., that are often interposed between integrated circuits on a board. In addition, facilities to perform internal test of a mixed-signal chip can be provided. This option is not mandatory.

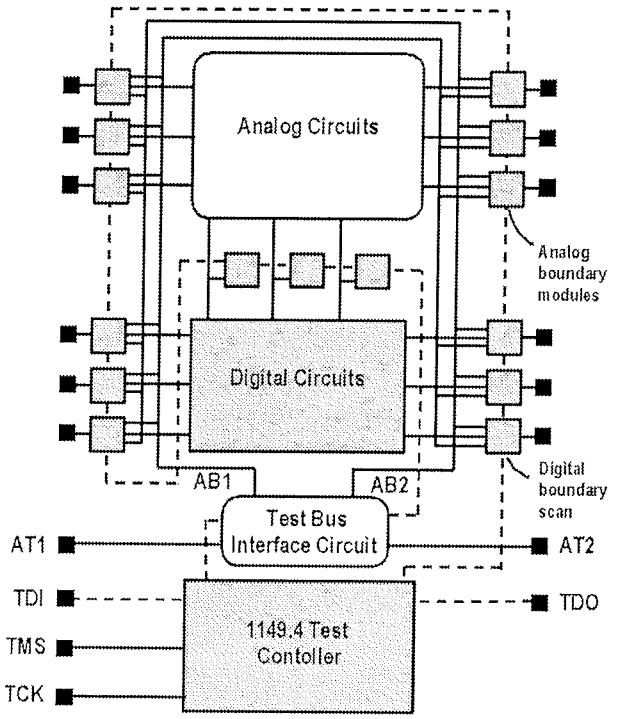

Figure 3: A schematic of a chip complying to IEEE Standard 1149.4

IEEE Standard 1149.4 can be regarded as an extension of IEEE Standard 1149.1. The 1149.4 extensions are analog boundary modules (ABMs) on analog functional pins accessed via internal analog test bus (AB1, AB2). The bus is connected to the Analog Test Access Port (ATAP) through the Test Bus Interface Circuit (TBIC). Digital pins have boundary cells as specified in IEEE Standard 1149.1. A schematic of a chip with included IEEE Standard 1149.4 test infrastructure is shown in Figure 3.

Four mandatory instructions are prescribed: Sample/Preload, Bypass and Extest (since the digital part is compliant with IEEE Standard 1149.1) and Probe. The Probe instruction allows analog pins to be monitored on the analog bus AB2, and/or stimulated from the analog bus AB1 while the chip is operating in its normal operation state.

2.3 Standard for Embedded Core Test

SoC design integrates large reusable blocks (i.e. cores) that have been designed and verified in earlier applications in practice. Embedded cores provide a wide range of functions, like CPUs, DSPs, interfaces, controllers, memories, and others. The cores put together in a SoC normally originate from different core providers. In order to protect their intellectual property core providers do not completely reveal design and implementation details which makes the problem of SoC testing rather challenging to the core user (i.e., SoC designer). On the other hand, correct operation of a core in the target SoC is of interest of both core user and core provider. In order to provide an independent openly defined design-for-testability method for integrated cir-

cuits containing embedded cores, an initiative to develop a standard has been taken by the IEEE P1500 Working Group, /7/.

The main entity of the test architecture defined by IEEE Standard P1500 is a *test wrapper* placed around each core of a SoC. Test wrapper provides interface between the embedded core and its environment. For testing a core, a test source generating test vectors and a test sink collecting the test responses must be provided. Test access mechanism (TAM) transports test vectors from the source to the core and test responses from the core to the test sink. It also allows testing of interconnects between SoC cores. Standard prescribes mandatory serial TAM and allows optional user-defined parallel TAMs.

The test wrapper, shown in Figure 4, connects the terminals of the core to the rest of SoC during the normal operation and to the test access mechanism in the test mode. Wrapper operation is controlled by a set of control and clock signals provided at the Wrapper Interface Port (WIP). WIP also includes Wrapper Serial Input (WSI) and Wrapper Serial Output (WSO) which are used to shift-in and shift-out serial test data. Test wrapper contains the following mandatory registers:

- wrapper instruction register (WIR) which is similar to IEEE 1149.1 instruction register and controls the operation of the wrapper. WIR receives instructions via wrapper serial input WSI.
- wrapper boundary register (WBR) to which the core functional terminals are connected. It is a serial shift register similar to the IEEE 1149.1 boundary-scan register.
- bypass register which is similar to IEEE 1149.1 bypass register. It is used to bypass the WBR. In a single scan path configuration, bypass registers enable to skip out the WBRs of the cores that are not being tested.

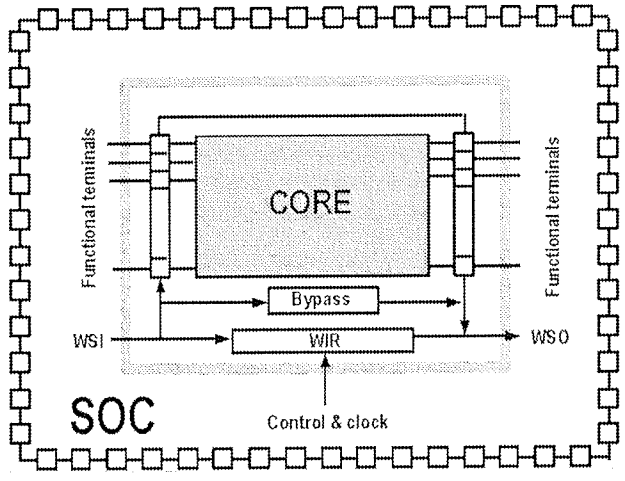

Figure 4: IEEE Standard 1500 test wrapper structure

Core-internal and core-external tests can be performed. Core-internal test is based on the test information that the core user gets from the core provider. It may consist of the application of test patterns within a specified test protocol, or of initiation of a built-in self-test of the core. Core-external test checks external connections between the cores and additional glue logic designed by the SoC integrator.

For the core-internal tests, test stimuli are provided via TAM to wrapper boundary at the core input terminals and test results are read via TAM from the wrapper boundary at the core output terminals. For the core-external tests, initial logical values are set-up via TAM at the wrapper boundary at the core output terminals and results are observed at the wrapper boundary at the core input terminals.

IEEE Standard P1500 prescribes three mandatory instructions: WS_BYPASS (which places wrapper bypass register between the WSI and WSO of the wrapper), WS_EXTEST (which allows testing of off-core circuitry and interconnections between cores) and Wx_INTEST (a user specified core test instruction).

2.4 Applications in practice

IEEE Standard 1149.1 is widely accepted standard supported by semiconductor industry and EDA tool providers. Since its introduction, the availability of devices conforming to the standard has increased steadily. Boundary-scan is an efficient technique for detecting and localizing manufacturing faults such as shorts, opens and component misplacements. The same test infrastructure is used to support built-in self-test (BIST) capabilities of complex devices. Extensive number of papers and technical reports are available on the web. For the newcomers, introductory book on boundary-scan /8/ may prove advantageous. Another major application of the 1149.1 boundary-scan infrastructure is the so-called In-System Configuration (ISC). ISC is the ability to load configuration data into a programmable device, such as a CPLD or a FPGA, via boundary-scan path. Standardization efforts in this area resulted in the IEEE 1532 In-System Configuration of Programmable Devices Standard /9/, approved in late 2000.

While the use of IEEE 1149.1 has become a prevalent solution for board and system manufacturing test, its analog counterpart IEEE 1149.4 still lacks the support of major electronic manufacturers. The absence of IEEE 1149.4 compatible devices prevents the designers to include a standardized mixed-signal test structure into their systems. So far, only a few experimental test chips supporting the standard have been reported /10/, /11/, /12/. On the other hand, the standard attracted the attention in research and academia. Beside the introductory book /13/, different test and measurement methods using IEEE 1149.4 test infrastructure have been proposed /14/ - /17/.

IEEE Standard P1500 is about to enter ballot process in the following months hence solutions in compliance with the standard could not yet be reported. But according to the expressed interest of core providers and SoC designers we can expect that the standard will gain wide support

in practice. Recently, numerous papers have been published on P1500 related issues in the proceedings of the International Test Conferences and the DATE Conferences. Papers /18/ - /22/ can serve as starting points for further reading on this subject.

Described standards are not stand-alone solutions. They are combined together with local DFT solutions to provide an efficient test. The IEEE Standard P1500 test wrapper, for example, provides means to perform internal core test via the scan chains originally implemented in the given core.

Application of DFT standards in practice is, of course, subject to a thorough economic analysis. However, when assessing the trade-off of a given DFT solution, testing should be regarded primarily as a cost-avoidance strategy. The well-known "Rule of Ten" indicates that the cost to locate a fault increases about ten times at each subsequent testing stage. A DFT solution that facilitates the location of faults at earlier testing stages reduces the product cost. The author and his research group share the experience that even a simple awareness of the DFT principles contributes to the system's testability as well as dependability features /23/.

3. Advanced embedded test approaches

The basic principle of embedded test is the generation of test stimuli and analysis of test results on the unit-under-test instead of using for this purpose an external ATE. Generation of test stimuli and collection of test results is specific to the type of the functional block under test.

For testing digital logic, pseudo-random pattern generator (PRPG) as stimuli generator and multiple-input signature register (MISR) for collection and compression of test results are normally employed. The pioneering work on signature analysis technique of R.A.Frohwerk /24/ has been followed by a vast number of papers exploring theoretical limits of pattern generation and compaction by this technique as well as different possibilities of its application in practice.

Embedded memories represent another type of functional block that requires specific test solutions. Conventional ad-hoc methods use either additional logic to route the embedded memory inputs and outputs to the external pins of the chip or place a scan chain around the embedded memory for shifting in and out the test patterns. The first approach is not adequate due to extensive routing of extra interconnects and to the restrictions in pin count of the chip while the second exhibits prohibitive test time. An alternative way is memory BIST approach /25/ with on-chip (or on-board) generation of test patterns and compression of test results. The requirement of generating deterministic sequences of test patterns (i.e., marching test pattern) for testing target memory structures resulted in different test algorithms. Specific features of test problems and solutions have made embedded memory test a unique research area.

Mixed-signal functional blocks are another group of system parts that require different embedded test approaches. This heterogeneous group calls for specific measurement-based solutions completely different from those described so far. A concise introduction on this subject is the book written by M.Burns and G.W.Roberts /26/. Any further discussion on this topic is, however, beyond the scope of this paper.

For any embedded test solution, either at chip or at board level, it is advantageous to provide test data input/output via standardized test port. In this way, communication with external tester or implementation of system test is considerably simplified. In addition, implementation of local embedded test solutions in the frame of standard test infrastructure complying to previously described DFT standards allows portability and reuse of embedded tests at higher system levels.

As mentioned before, IEEE Standard 1149.1 and 1149.4 test infrastructure originally supports low speed interconnect test. However, with miner modifications of boundary-scan cells and small additional control logic it is possible to perform at-speed interconnect test /3/. Besides, novel techniques that exploit IEEE Standard 1149.4 test structures in high frequency measurements have been recently reported /12/, /27/, /28/.

4. Conclusion

Conventional test techniques are inadequate for testing complex modern SoCs, boards and systems due to the low bandwidth and low test speed, limited access of internal test points resulting in increased test time and test cost. Alternative approaches with embedded test solutions provide several advantages including cost-effective at-speed test, increased fault coverage and reuse of device test at the board or system level. In practice, most current test solutions rely on DFT standards. Basic knowledge of their principles and possible use of their test infrastructure is imperative for modern chip design. The paper gives a brief overview of the above issues and offers a list of related references.

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