CORE-BASED DESIGN WITH PARASITIC-AWARE APPROACH FOR MEDIUM POWER AMPLIFIER AT 900 MHz, 2.4 GHz, 3.5 GHz AND 5.85 GHz

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Key words: medium power amplifier, parasitic aware approach, RFIC, MMIC

Abstract: Practical core-based design suitable for medium power amplifier (MPA) is presented. The core circuit is developed and applied at 0.9 GHz, 2.4 GHz, 3.5 GHz and 5.85 GHz. Parasitic-aware design flow is introduced in the whole approach. 5.85 GHz MPA achieves a P1dB of 16.5 dBm, PAE of 15.8% and gain of 4.5 dB at the 12 dBm power input under a low power supply of 2.5V. The maximum current, I_{max} is 77 mA and the power consumption of the device is 192.50 mW. 3.5 GHz MPA achieves a P1dB of 18.2 dBm, PAE of 26.5% and gain of 7.98 dB at the 10.2 dBm power input under a low power supply of 3.0V. The maximum current, I_{max} is 79 mA and the power consumption of the device is 237 mW. 2.4 GHz MPA achieves a P1dB of 17 dBm, PAE of 20.1% and gain of 7.0 dB at the 10 dBm power input under a low power supply of 3.0V. The maximum current, I_{max} is 79 mA and the power consumption of the device is 237 mW. 0.9 GHz MPA achieves a P1dB of 14.2 dBm, PAE of 11% and gain of 4.2 dB at the 10 dBm power input under a low power supply of 3.0V. The maximum current, I_{max} is 79 mA and the power consumption of the device is 237 mW. 0.9 GHz MPA achieves a P1dB of 14.2 dBm, PAE of 11% and gain of 4.2 dB at the 10 dBm power input under a low power supply of 3.0 V. The maximum current, I_{max} is 79 mA and the power consumption of the device is 237 mW. 0.9 GHz MPA achieves a P1dB of 14.2 dBm, PAE of 11% and gain of 4.2 dB at the 10 dBm power input under a low power supply of 3.0 V. The maximum current, I_{max} is 79 mA and the power consumption of the device is 237 mW. Lastly, simulated results almost match the measurement results shows the advantages of applying parasitic information to the core circuit for MPA designs and the effectiveness of corebased design approach in Radio Frequency Integrated Circuit (RFIC) and Monolithic Microwave Integrated Circuit (MMIC).

Načrtovanje ojačevalnikov srednjih moči upoštevajoč parazitne vplive pri frekvencah 900MHz, 2.4GHz, 3.5GHz in 5.85GHz

Kjučne besede: ojačevalniki srednjih moči, upoštevanje parazitnih vplivov, RFIC, MMIC

Izvleček: V prispevku predstavimo praktično izvedbo načrtovanja ojačevalnikov srednjih moči (MPA-Medium Power Amplifier). Osrednje vezje smo razvili in uporabili pri frekvencah 0.9 GHz, 2.4 GHz, 3.5 GHz and 5.85 GHz. Metode načrtovanja so take, da ves čas vodimo računa o parazitnih vplivih. Pri 5.85 GHz MPA smo dosegli P1dB pri 16.5 dBm, PAE 15.8% in ojačanje 4.5 dB pri 12 dBm vhodne moči in pri nizki napajalni napetosti 2.5V. Največji tok, I_{max} je 77mA, poraba moči pa 192.5mW. Pri 3.5 GHz MPA smo dosegli P1dB pri 18.2 dBm, PAE 26.5% in ojačanje 7.98 dB pri 10.2 dBm vhodne moči in pri napajalni napetosti 3.0V. Največji tok, I_{max} je 79mA, poraba moči pa 237mW. Pri 2.4 GHz MPA smo dosegli P1dB pri 17 dBm, PAE 20.1% in ojačanje 7.0 dB pri 10.2 dBm vhodne moči in pri napajalni napetosti 3.0V. Največji tok, I_{max} je 79mA, poraba moči pa 237mW. Pri 2.4 GHz MPA smo dosegli P1dB pri 14.2 dBm, PAE 11% in ojačanje 4.2 dB pri 10 dBm vhodne moči in pri napajalni napetosti 3.0V. Največji tok, I_{max} je 79mA, poraba moči pa 237mW.

Merjeni rezultati se ujemajo s simuliranimi, kar potrjuje pravilen pristop k izvedbi MPA z upoštevanjem parazitnih vplivov pri načrtovanju radiofrekvenčnih (RFIC) in mikrovalovnih (MMIC) integriranih vezij.

1. Introduction

The wireless communication industry has grown rapidly in recent years. The growing Wireless LAN (WLAN) has generated increasing interest in technologies that enable higher data rates and capacity than initially deployed systems. LAN applications have driven the demand for personal wireless communications terminals, and these items need to be low-operating voltage and small size /1/. Power amplifiers among these terminals play a very important role in these systems. So, the application ambit this power amplifier is the key component for researching the advance systems of WLAN and other wireless network systems.

The Gallium Arsenide (GaAs) Pseudomorphic High Electron Mobility Transistor (PHEMT) has good performances on the frequency range, noise figure, output power, and high efficiency with low distortion /2, 3, 4, 5/. Because of its superior performance over the metal oxide semiconductor (MOS) transistors, GaAs transistors have been used extensively to build the Radio Frequency (RF) power amplifiers and play an important role in the wireless communications. PHEMT power amplifiers are making serious inroads into handset cellular (800 MHz to 2.3 GHz) and Wireless LAN (WLAN) (2.4 GHz to 5.85 GHz) applications /6/. GaAs technology has lower R&D cost than CMOS R&D cost is another factor which lures companies to use the technology in power amplifier design /7/.

In system level design, RF platform-based design is normally applied to reduce design cycles /8/. It is often for designing a multi-band, multi-mode IC, reconfigurable reference platform design approach is normally employed /9/. Minimum number of sub-blocks and definition common block is very much useful for first time right IC. Due to uncertainty in layout and parasitic, high frequency integrated circuit design normally needs number of design cycles. Parasitic-aware design flow /10/ is introduced to reduce number of design iterations. The combination of platformbased and parasitic-aware approach could reduce the design cycles and offer flexible block for first time right IC. This approach is very useful for highly integrated multistandard application integrated RF Front-end silicon-based design /11/. As GaAs technologies become acceptable for RFIC application /7/, the approach can also be applied here.

The design of core circuit and the final design for a 5.85 GHz, 3.5 GHz, 2.4 GHz single-ended medium power amplifier (MPA) for wireless LAN application and 0.9 GHz single-ended medium power amplifier for handset cellular are described in details in this work.

This paper is organized as follows. We first give an introduction to the application of MPA, the technology and the design approach. The following section details out the methodology, design and simulation results. Finally, experimental results and conclusion are discussed in the last two sections.

2. Design

2.1 Design Methodology

Typical MMIC or RFIC design process is to start with topology analysis with respect to specifications. Topology is then simulated at schematic level to verify the performance against the specification. The design is then convert into the layout and post-layout simulation is done to verify the performance against the schematic simulation. If the performance is not similar to the specifications, the design layout has to be modified. The process is repeated until the specifications are met. Multi-band RFIC designs use many approaches; wideband design, parallel design and single design with flexible matching components. This work discusses core-based design approach which can also deliver Multi-band RFIC.

The design flow in Figure 1 is used in this work to give full considerations for the effects that parasitic have on circuit performance. A common block or core circuit which satisfies the specifications at all interested frequencies must be figured out first /8/. The core schematic circuit must be simulated with layout with known parasitic performance. This approach will reduce the design iterations.



Fig. 1: Parasitic-Aware Design Flow /10/

2.2 Core Circuit Design



Fig. 2: Core circuit.

From Figure 2, resistor R_F forms the feedback and capacitor C_F is added to allow for independent biasing of the gate and drain of the transistor. C_F can normally be chosen so that it is large enough to be a short circuit over the frequency of interest. In addition, the effect of feedback is to make the input and the output impedances more convenient for matching. Q is depletion-mode transistor which requires negative biasing voltage, R_s is used to set the biasing condition. C_s is used to short the R_s at all interested frequencies. The configuration of the core circuit is very similar to shunt-series amplifier.

From Figure 2, the closed-loop gain, A_V

$$A_{F} = -\frac{1}{\left(\frac{G_{F}(1+\frac{1}{A_{OL}})}{G_{S}} + \frac{1}{A_{OL}}\right)}$$
(1)

where G_F , G_S , A_{OL} is conductance of feedback resistance, conductance of source resistance and open-loop gain respectively. The closed-loop gain will be equal to an open-loop gain if G_F approaches zero. In this case, the open loop gain is referring to transistor gain without feedback topology. An amplifier with the resistor feedback can achieve self matching /13/.

Details of high frequency small-signal analysis can be found in Thomas Lee's book /12/. This topology offers wide bandwidth /13/, which is suitable candidate for the MPA at different frequency.



Fig. 3: Core circuit simulation results

From Figure 3, the performance of core circuit is compared. S(1,1), S(1,2), S(2,1) and S(2,2) are partial schematic level simulation results. The layout information is added to circuit by adding transmission line model between transistor source and capacitor. S(5,5) S(5,6), S(6,5) and S(6,6) are schematic simulation results. From Figure 3, it can be concluded that parasitic information does affect the input and output reflection coefficient of the core circuit. The input impedance and output impedance of the core circuit is important information for MPA design. All circuits use active and passive models from the foundry with transistor; number of finger (NOF) = 10, unit gate width (UGW) = 100 μ m, C_F = 8 pF, C_s = 2 pF, R_F = 500 Ω and R_s = 10 Ω . The core circuit with parasitic information is modeled as modified-transistor and later used in MPA design.

2.3 Medium Power Amplifier Design

The complete schematic designed MPA are shown in Figures 4 and 5 where L_G, L_S, L_D and L_O are all implemented on-chip. The inductors L_G and L_S are chosen to provide the desired input impedance. The inductor L_D is a current source for the MPA and used for output power matching. The capacitor C_{in} at the input is used for input matching. The capacitor C_C at the output plays a role for both DC block and output matching. The capacitor C_O is used for network matching. The outputs are matched for high compression point, P1dB.



Fig. 4: Circuit schematic of the PHEMT single-ended medium power amplifier for RF frequency of 2.4 GHz, 3.5 GHz, and 5.85 GHz.



Fig. 5: Circuit schematic of the PHEMT single-ended medium power amplifier for RF frequency of 0.9 GHz.

2.3.1 Result & Discussion

The single-ended medium power amplifiers are shown in Figure 4 and 5 are simulated in $0.15\mu m$ GaAs PHEMT process technology using ADS simulator /14/. The supply voltage, V_{DD} for this simulation is 2.5 V to 3.0 V.

i) MPA at 5.85 GHz

The small-signal performance of the single-ended MPA is shown in Figure 6 over 1 to 6 GHz. The linear gain (S(21)) obtained is 6.3 dB, S(12) is -14.8 dB, input return loss is 20.6 dB and output return loss is 5.4 dB at a frequency of 5.85 GHz and V_{DD} s 2.5 V.

Figure 7 shows a stability factor, K as a function of frequency for this single-ended MPA. At 5.85 GHz, a stability factor, K for this device is 1.172. The MPA is in unconditionally stable condition due to the stability factor for the MPA is higher than 1 at the whole range of frequency.



Fgi. 6: Gain, input return loss and output return loss as a function of frequency for medium power amplifier at 5.85 GHz.



Fig. 7: Stability factor, K of medium power amplifier at 5.85 GHz.



Fig. 8: Output power, power added efficiency and power gain versus input power for medium power amplifier at 5.85 GHz.

Figure 8 shows the output power, power gain and the power added efficiency, PAE as a function of input power, respectively. The MPA has an output power of 16.5 dBm at 1dB gain compression (P1dB), a power gain of 4.5 dB and the power added efficiency (PAE) of 15.8% for an input power, P_{in} of 12 dBm.

Figure 9 shows the maximum available gain, MAG, associated power gain and gain as a function of frequency for the simulated PHEMT medium power amplifier. At 5.85 GHz, the MAG is 8.04 dB and the associated power gain is 7.993



Fig. 9: Maximum available gain, MAG, associated power gain and gain of medium power amplifier at 5.85 GHz.

dB. The MAG is the maximum available gain at all frequencies with the output condition matched to 50 Ohm.

ii) MPA at 3.5 GHz

The small-signal performance of the single-ended MPA is shown in Figure 10 over 1 to 6 GHz. The linear gain (S(21)) obtained is 11.4 dB, S(12) is -18.8 dB, input return loss is 18.1 dB and output return loss is 10.4 dB at a frequency of 3.5 GHz and V_{DD} is 3.0 V.





Figure 11 shows a stability factor, K as a function of frequency for this single-ended MPA. At 3.5 GHz, a stability factor, K for this device is 1.305. The MPA is in unconditionally stable condition due to the stability factor for the MPA is higher than 1 at the whole range of frequency.

Figure 12 shows the output power, power gain and the power added efficiency, PAE as a function of input power, respectively. The MPA has an output power of 18.2 dBm at 1dB gain compression (P1dB), a power gain of 7.98 dB and the power added efficiency (PAE) of 26.5% for an input power, P_{in} of 10.2 dBm.

Figure 13 shows the maximum available gain, MAG, associated power gain and gain as a function of frequency for



Fig. 11: Stability factor, K of medium power amplifier at 3.5 GHz.



Fig. 12: Output power, power added efficiency and power gain versus input power for medium power amplifier at 3.5 GHz.



Fig. 13: Maximum available gain, MAG, associated power gain and gain of medium power amplifier at 3.5 GHz.

the simulated PHEMT medium power amplifier. At 3.5 GHz, the MAG is 11.8 dB and the associated power gain is 11.5 dB. The MAG is the maximum available gain at all frequencies with output condition matched to 50 Ohm.

iii) MPA at 2.4 GHz

The small-signal performance of the single-ended MPA is shown in Figure 14 over 1 to 6 GHz. The linear gain (S(21)) obtained is 10.9 dB, S(12) is -20.5 dB, input return loss is 6.1 dB and output return loss is 5.6 dB at a frequency of 2.4 GHz and V_{DD} is 3.0 V.



Fig. 14: Gain, input return loss and output return loss as a function of frequency for medium power amplifier at 2.4 GHz.

Figure 15 shows a stability factor, K as a function of frequency for this single-ended MPA. At 2.4 GHz, a stability factor, K for this device is 1.233. The MPA is in unconditionally stable condition due to the stability factor for the MPA is higher than 1 at the whole range of frequency.



Fig. 15: Stability factor, K of medium power amplifier at 2.4 GHz.



Fig. 16: Output power, power added efficiency and power gain versus input power for medium power amplifier at 2.4 GHz.

Figure 16 shows the output power, power gain and the power added efficiency, PAE as a function of input power, respectively. The MPA has an output power of 17.0 dBm at 1dB gain compression (P1dB), a power gain of 7.0 dB and the power added efficiency (PAE) of 20.1% for an input power, P_{in} of 10 dBm.



Fig.e 17: Maximum available gain, MAG, associated power gain and gain of medium power amplifier at 2.4 GHz.

Figure 17 shows the maximum available gain, MAG, associated power gain and gain as a function of frequency for the simulated PHEMT medium power amplifier. At 2.4 GHz, the MAG is 12.79 dB and the associated power gain is 11.68 dB. The MAG is the maximum available gain at all frequencies with the output condition matched to 50 Ohm.

iv) MPA at 0.9 GHz

The small-signal performance of the single-ended MPA is shown in Figure 18 over 1 to 6 GHz. The linear gain (S(21)) obtained is 10.1 dB, S(12) is -19.8 dB, input return loss is 13.4 dB and output return loss is 12.1 dB at a frequency of 0.9 GHz and V_{DD} is 3.0 V.



Fig. 18: Gain, input return loss and output return loss as a function of frequency for medium power amplifier at 0.9 GHz.

Figure 19 shows a stability factor, K as a function of frequency for this single-ended MPA. At 0.9 GHz, a stability factor, K for this device is 1.536. The MPA is in unconditionally stable condition due to the stability factor for the MPA is higher than 1 at the whole range of frequency.

Figure 20 shows the output power, power gain and the power added efficiency, PAE as a function of input power, respectively. The MPA has an output power of 14.2 dBm at 1dB gain compression (P1dB), a power gain of 4.2 dB and the power added efficiency (PAE) of 11% for an input power, P_{in} of 10 dBm.



Fig. 19: Stability factor, K of medium power amplifier at 0.9 GHz.



Fig. 20: Output power, power added efficiency and power gain versus input power for medium power amplifier at 0.9 GHz.



Fig. 21: Maximum available gain, MAG, associated power gain and gain of medium power amplifier at 0.9 GHz.

Figure 21 shows the maximum available gain, MAG, associated power gain and gain as a function of frequency for the simulated PHEMT medium power amplifier. At 0.9 GHz, the MAG is 10.6 dB and the associated power gain is 9.5 dB. The MAG is the maximum available gain at all frequencies with the output condition matched to 50 Ohm.

Table 1 shows the summary of MPA performance for this work at different frequency. It is also shown that poor return losses at some frequencies could be attributed due to insufficient matching at the input and output of the MPA.

Parameter	This work			
Frequency	5.85	3.5	2.4	0.9
(GHz)				
S21 (dB)	4.5	11.4	10.9	10.1
PAE (%)	15.8	26.5	20.1	11
P1dB (dBm)	16.5	18.2	17.0	14.2
S12 (dB)	-14.8	-18.8	-20.5	-19.8
S11 (dB)	-20.6	18.1	6.1	13.4
S22 (dB)	-5.4	10.4	5.6	12.1
Voltage	2.5	3.0	3.0	3.0
Supply (V)				
$L_{g}(nH)$	2.16	2.16	2.16	10.95
$C_{in}(pF)$	n/a	n/a	n/a	0.8
$L_{s}(nH)$	0.372	0.372	0.372	0.372
$L_{D}(nH)$	5.288	5.288	4.128	5.288
$C_C(pF)$	1	4.2	7.7	4.5
L _O (nH)	1.35	1.65	2.436	5.288
$C_{O}(pF)$	0.76	1	1.4	2.1
Application	802.11a	802.16	802.11a/b/g	Handset
	Wireless	WiMAX	Wireless	cellular
	LAN		LAN	

Table 1: Summary of single-ended MPA performance.



Fig. 22: Core circuit microphotograph



Fig. 23: 5.85 GHz MPA microphotograph

Therefore more design optimization /15/ is required to improve the performance of the MPA in this work.

Some of the passive devices such as capacitors and inductors have been characterized and presented in confer-



Fig. 24: 3.5 GHz MPA microphotograph



Fig. 25: 2.4 GHz MPA microphotograph



Fig. 26: 0.9 GHz MPA microphotograph

ence /16, 17/. MPA of 5.85 GHz results have also been presented in a conference /18/.

3. Experimental Results

Figure 22 shows photo of fabricated core circuit while Figure 23, 24, 25, 26 shows 5.85 GHz, 3.5 GHz, 2.4 GHz and 0.9 GHz MPA microphotographs respectively. A standard on wafer measurement methodology is used in characterizing the core circuit. In the S-Parameter results (Figure 27), the orders of the charts are S11 and S22 (Unit Smith Chart), S21 Magnitude (dB), and S12 Magnitude (dB). The S-parameter measurement is performed in the



Fig. 27: Simulation and measurement data for core circuit.

frequency range from 2 GHz to 8 GHz and the bias conditions is 2.5 V of drain voltage, V_{DS} and a gate voltage, V_{GS} is 0 V. The drain current, I_{D} is 83 mA.

It can be seen from Figure 27, the partial schematic layout simulation (S(3,3), S(4,3), S(3,4) and S(4,4)) is almost similar to the measurement results. Unfortunately due to test equipments issue, no MPA measurement has been made.

4. Conclusion

A core-based and parasitic-aware design flow is presented and MMIC designs using the same core circuit for all interested frequencies are also presented. Measurement results of core circuit very much similar to the parasiticaware schematic simulation result, this has shown the potential of the approach in designing multi-standard and multiapplication RFIC and MMIC.

A single-ended medium power amplifier using 0.15 μ m GaAs power PHEMT process technology with a gate width of 100 μ m and 10 fingers is presented. A 5.85 GHz MPA achieved a P1dB of 16.5 dBm, PAE of 15.8% and gain of 4.5 dB at the 12 dBm power input under a low power supply of 2.5V. The maximum current, I_{max} is 77 mA and the power consumption of the device is 192.50 mW. Other results; a linear gain (S21) of 6.3 dB, input return loss of 20.6 dB, output return loss of 5.4 dB and a stability factor, K of 1.172 at RF frequency of 5.85 GHz. This MPA is suitable for IEEE 802.11a wireless LAN applications.

3.5~GHz MPA achieved a P1dB of 18.2 dBm, PAE of 26.5% and gain of 7.98 dB at the 10.2 dBm power input under a low power supply of 3.0V. The maximum current, I_{max} is 79 mA and the power consumption of the device is 237 mW. Other results; a linear gain (S21) of 11.4 dB, S(12) of

-18.8 dB, input return loss of 18.1 dB, output return loss of 10.4 dB and a stability factor, K of 1.305 at RF frequency of 3.5 GHz. This MPA is suitable for IEEE 802.16 WiMAX applications.

2.4 GHz MPA achieved a P1dB of 17 dBm, PAE of 20.1% and gain of 7.0 dB at the 10 dBm power input under a low power supply of 3.0V. The maximum current, I_{max} is 79 mA and the power consumption of the device is 237 mW. Other results; a linear gain (S21) of 10.9 dB, S(12) of -20.5 dB, input return loss of 6.1 dB, output return loss of 5.6 dB and a stability factor, K of 1.233 at RF frequency of 2.4 GHz. This MPA is suitable for IEEE 802.11a/b/g wireless LAN applications.

0.9 GHz MPA achieved a P1dB of 14.2 dBm, PAE of 11% and gain of 4.2 dB at the 10 dBm power input under a low power supply of 3.0 V. The maximum current, I_{max} is 79 mA and the power consumption of the device is 237 mW. Other results; a linear gain (S21) of 10.1 dB, S(12) of - 19.8 dB, input return loss of 13.4 dB, output return loss of 12.1 dB and a stability factor, K of 1.536 at RF frequency of 0.9 GHz. This MPA is suitable for handset cellular applications.

Even though there is no measurement on MPA designs, authors believe based on the core circuit measurement results the targeted simulation results of MPA can be achieved.

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