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Design of a Low-Power Phase-Frequency Detector and Gain-Boosting Charge Pump for GHz-Range Applications in 180-nm CMOS Technology

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Abstract: Phase-Frequency Detector (PFD) and Charge Pump (CP) are crucial components in Phase-Locked Loops (PLL) and Delay-Locked Loops (DLL), significantly impacting synchronization accuracy and system stability. In this paper, a new PFD based on dynamic logic with a minimal number of devices is designed, providing low delay and proper logic output levels. Additionally, a novel CP employing the gain-boosting technique and utilizing a cascode amplifier is proposed, achieving higher DC-gain and better current matching. The proposed design aims to minimize power consumption to the microwatt level, reduce circuit area, and achieve an operating frequency up to 3 GHz. Simulation results in 180-nm CMOS technology using Cadence software demonstrate that the proposed circuit offers lower power consumption, smaller area, and improved dynamic performance compared to conventional designs, making it well-suited for PLL and DLL applications in high-frequency communication systems.

Keywords: Phase-Frequency Detector (PFD), Charge Pump (CP), Gain Boosting, Low Power, Current Matching.

Zasnova fazno-frekvenčnega detektorja nizke moči in polnilne črpalke za povečanje ojačenja za aplikacije v območju GHz v 180-nm tehnologiji CMOS

Izvleček: Detektor fazne frekvence (PFD) in polnilna črpalka (CP) sta ključni komponenti v fazno zaklenjenih zankah (PLL) in zakasnitveno zaklenjenih zankah (DLL), ki pomembno vplivata na natančnost sinhronizacije in stabilnost sistema. V članku je predstavljen nov PFD, zasnovan na dinamični logiki z minimalnim številom naprav, ki zagotavlja nizko zakasnitev in ustrezne logične izhodne ravni. Poleg tega je predlagan nov CP, ki uporablja tehniko povečanja ojačitve in kaskodni ojačevalnik, s čimer se doseže višja ojačitev DC in boljše prilagajanje toka. Predlagana zasnova ima za cilj zmanjšati porabo energije na raven mikrovatov, zmanjšati površino vezja in doseči delovno frekvenco do 3 GHz. Rezultati simulacije v 180-nm CMOS tehnologiji z uporabo programske opreme Cadence kažejo, da predlagano vezje ponuja nižjo porabo energije, manjšo površino in izboljšano dinamično zmogljivost v primerjavi s konvencionalnimi zasnovami, zaradi česar je primerno za PLL in DLL aplikacije v visokofrekvenčnih komunikacijskih sistemih.

Ključne besede: Detektor faze in frekvence (PFD), polnilna črpalka (CP), povečanje ojačitve, nizka poraba energije, prilagajanje toka

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1 Introduction

Nowadays, delay-locked loops (DLLs) are widely used in various applications such as local oscillators and clock generators. With the continuous scaling of CMOS technology and the reduction in transistor dimensions, both the number of transistors per chip and the operating frequency of circuits have significantly increased.

This increase in operating frequency and transistor count has resulted in a significant clock skew problem, especially in high-performance systems [1–5]. Additionally, power consumption is a crucial factor, particularly in portable devices where it must be carefully considered. Phase-locked loops (PLLs) and DLLs are widely employed in clock and data recovery systems, DRAM interfaces, and high-performance microprocessors to mitigate clock skew. PLLs are relatively complex systems, as their loop bandwidth can vary significantly due to process, voltage, temperature, and load (PVTL) variations. Moreover, the voltage-controlled oscillator (VCO) accumulates jitter in oscillation cycles due to its feedback structure. DLLs are preferred over PLLs due to their simpler design, lower jitter, reduced power consumption, and smaller area.

DLLs offer several advantages in telecommunications systems [6–10]. They reduce clock jitter, which is essential for high-speed and high-precision applications, and typically consume less power than PLLs, making them suitable for energy-limited devices. Their simpler architectures allow rapid deployment and cost-effective implementation. Additionally, DLLs provide robust performance against process and temperature variations, can efficiently operate at high frequencies by compensating for delays, and enable precise signal synchronization to improve data quality and reduce timing errors. In multipath networks, DLLs help synchronize signals arriving from multiple paths, thereby reducing interference and enhancing overall signal quality.

These advantages make DLLs an efficient and suitable choice for telecommunications systems with specific needs such as high speed, precise timing, and low power consumption. Conventional analog DLLs provide good performance in terms of clock skew and jitter; however, they suffer from high power consumption and large silicon area [11–12]. On the other hand, digital DLLs have smaller chip area and lower power consumption. Additionally, their locking time is faster, but they suffer from poor jitter performance [13-15]. The block diagram of the DLL is shown in Figure 1. Typically, there are four main blocks for DLL operation. The first and second blocks are the Phase Frequency Detector (PFD) and Charge Pump (CP), respectively. The third block is the Voltage-Controlled Delay Line (VCDL). The final block is the Loop Filter (LP) [3-5].

Regarding the operation of the PFD, it should be noted that when the signal (V_{out} VCDL) is ahead of the rising edge of the reference input signal (Ref_CLK), the DOWN output is activated and generates a pulse proportional to the phase difference between (Ref_CLK) and (V_{out} VCDL), while the UP output remains zero. In the other case, when (V_{out} VCDL) is phase-lagged with respect to (Ref_CLK), the UP output is activated and the DOWN output stays at zero. When both signals are in phase, the PFD output has zero values.

The DLL employs a current-based charge pump architecture in which a MOSFET functions as a switching element. The objective is to convert the detected phase error into a corresponding current while minimizing the phase jitter caused by power supply fluctuations [10]. When the two signals are synchronized, the CP does nothing. When the PFD generates the UP or DOWN signal, the CP either supplies or sinks current to/from the LPF. The LPF uses the current from the CP to convert it into a voltage for adjusting the delay of the VCDL.

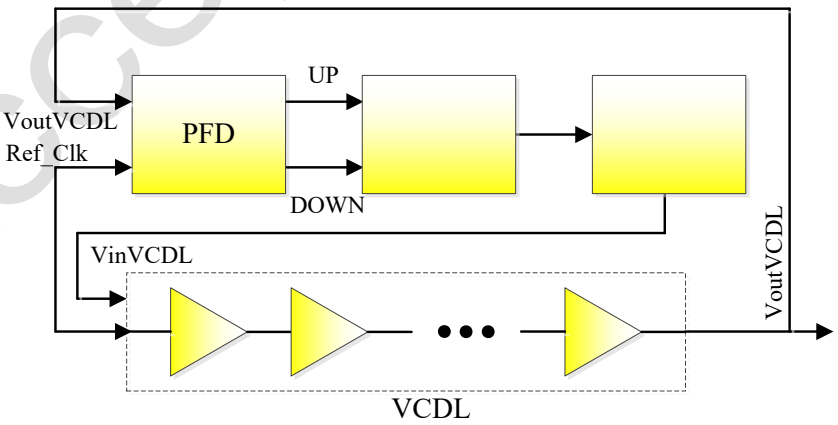


Figure 1. Block Diagram of the Delay-Locked Loop (DLL) [3].

Studies have been carried out in the field of PFD circuit design [1-13]. The paper [1] presents a design of a PFD in 180-nm technology using XOR and NAND gates. The power consumption of the PFD is 1310 µW when operating at a clock frequency of 500 MHz. The results are

compared with conventional current-mode logic designs, demonstrating that the proposed design achieves lower power consumption. The proposed PFD is a suitable circuit for low-power and high-speed systems. A low-power frequency multiplier based on a DLL is presented in [2]. The design is implemented in a 22 nm technology and achieves up to an 8-fold frequency multiplication. The proposed DLL incorporates a new, simple duty-cycle correction circuit and employs XOR logic for frequency multiplication. This circuit requires significantly less power and chip area compared to PLL circuits. To enhance the frequency lock range, a DLL circuit with a frequency-to-voltage converter (FVC) and a phase selection circuit is presented in [3]. To reduce power consumption, the circuit's bias current is kept at a low level. Simulation results show that the operating frequency range extends from 54 MHz to 250 MHz.

In [4], a phase selection circuit, a new PFD, and a modified voltage-controlled delay line are proposed to improve the lock range. The DLL presented in this paper also features a wide frequency range. A modified phase selection circuit is designed to allow the DLL to operate over a wide frequency range while addressing the issue of false locking. Additionally, a modified PFD is designed to reduce phase error and the dead zone. A DLL with a sequential approximate register circuit for achieving fast locking is proposed in [5]. To reduce power consumption, a loop state controller is proposed, which dynamically adjusts the operating states of the DLL according to the lock condition. When the loop locks, the path passing through the register enters sleep mode, and part of the circuit is deactivated in energy-saving mode. The paper [6] presents a quadrature voltage-controlled oscillator (QVCO) with a DLL for ultra-wideband (UWB) applications. A new DLL architecture is proposed to achieve low power consumption and low-noise performance. The system analysis of the delay-locked loop-based QVCO, including the transfer function and stability, is discussed. A fully digital DLL (ADDLL) with a frequency range from 3 MHz to 1.8 GHz and power consumption from 94 µW to 9.5 mW, using 65 nm technology, is presented in [7]. By using the proposed techniques, the chip area is only 0.0153 mm^2, and the operating frequency range extends up to 1.8 GHz. In the paper [8], a low-power DLL with a modified voltage-controlled delay cell (VCDC) is proposed. This modified VCDC is designed using a 130-nm CMOS technology. It is worth mentioning that the DLL with the proposed VCDC has a power consumption of 921.57 µW.

In the paper [9], the design of a low-power dynamic PFD is proposed. The dynamic PFD enables the DLL to detect phase error information in the form of high-frequency pulses, playing a key role in enhancing the overall performance of the DLL. The phase frequency detector is simulated in 180 nm technology with a supply voltage of 1.8 V. Simulation results of the proposed PFD block demonstrate a significant reduction in both area and power consumption, confirming the efficiency of the dynamic design. A low-power DLL-based data and clock recovery circuit is designed in this paper [10]. A standby filter is a new feature in this design. A level tracking technique is used for data recovery. The circuit is designed using Verilog HDL, and the layout is generated using Cadence. The chip area and total dynamic power dissipation of the circuit are 0.01 mm^2 and 799.86 µW, respectively, with a supply voltage of 1.8 V. In [11], an 8-bit SAR-based ADDLL operating from 500 MHz to 1.5 GHz is designed and simulated using 130 nm CMOS technology. The proposed ADDLL incorporates a novel digitally controlled delay line (DCDL) which offers excellent linearity in the SAR code–delay curve and low power consumption. Unlike other SAR-based ADDLLs, the proposed DCDL does not include a complex binary-to-thermometer decoder, resulting in reduced power dissipation and a smaller chip area. The architecture in [12] features a coarse-step TDC and an analog feedback loop for fine steps. A phase-blending technique using dual delay lines (DDL) enhances coarse time resolution without increasing the lock time. The proposed DLL functions within a clock frequency range of 0.6 GHz to 2 GHz, implemented in 65 nm CMOS technology. In [13], a Flip-flop PFD is considered, where flip-flops are constructed as an asynchronous sequential logic circuit. This approach effectively eliminates the false lock issue, also known as the harmonic input signal problem.

The article [14] presents a 360° phase detector for 2–18 GHz applications with 160% relative bandwidth, using a fixed delay line and double signal multiplication. The key innovation is a delay-line-based phase shift (90° ± 72°), easily adaptable to other technologies. The prototype achieves low phase errors (<±5°) and demonstrates high bandwidth and flexible integration. This article [15] proposes a low-cost method for phase detector measurement using quasi-synchronized RF generators and Arduino-based control. By alternating calibration and measurement, it compensates for phase drift and ensures high accuracy (±1°). The method was tested from 3–8 GHz, achieving final errors under ±2°. The article [16] presents a complementary mixing phase detector (CMPD) to enhance reference spur suppression in mm-wave PLLs without compromising the loop bandwidth. Unlike traditional RC filters, CMPD uses mutual harmonic rejection enhanced by foreground calibration. It also cancels charge injection and clock feedthrough without extra power consump-

tion, while supporting both frequency and lock detection. The paper [17] presents a 2.0–7.4 GHz 16-phase single-loop DLL with high phase accuracy and wide locking range. A cascode current-splitting charge pump is employed to reduce current mismatch and phase-delay errors. A novel lock detector addresses false and harmonic locking, extending detection range. Fabricated in 40-nm CMOS, the DLL achieves phase-delay errors as low as 0.5 ps and consumes 18.3 mW at 7.4 GHz, demonstrating high power efficiency and compact design.

In this paper, a novel dynamic PFD is introduced, utilizing dynamic logic with fewer devices. The proposed PFD offers high operating frequency and low power consumption. Subsequently, the charge pump (CP), employing a gain-boosting technique with excellent current matching, is presented. Section 2 provides a review of existing works in the field. In Section 3, the details of the proposed PFD and CP are discussed. Performance evaluations of the proposed circuits and a comparison of the results are presented in Section 4. Finally, Section 5 concludes the paper.

2 Proposed Circuits

In this section, we introduce the PFD and CP. The design approach and key considerations for both components are discussed in detail. First, the architecture of the PFD is described, highlighting its innovative features and how it addresses common issues such as power consumption. Next, the design of the CP is explained, focusing on its performance characteristics. Both components have been carefully engineered to ensure high accuracy and low power consumption in the overall system.

2.1 Proposed PFD Circuit

Figure 2 illustrates the circuit schematic of the proposed PFD, which is implemented using two switches and CMOS inverters. The PFD receives two input signals: the reference clock (IN) and the clock output from the VCDL, which serves as the second input clock (VCDL). These two clock inputs are compared to determine phase differences. The PFD generates two output signals: DOWN and UP, which are used to control the subsequent charge pump and loop filter in the DLL system [18-22]. The performance characteristics of the PFD are summarized in Table 1.

Table 1. PFD performance.

State	PFD outputs		PFD inputs
1	UP=0	DOWN=0	When both input signals match exactly
2	UP=0	DOWN=1	When the VCDL signal is ahead of the other input
3	UP=1	DOWN=0	When the IN signal precedes the other input
4	UP=1	DOWN=1	It cannot be done

The PFD circuit comprises three main components. The PFD circuit comprises three main components: Dynamic logic, Multiplexer, and Voltage Level Buffers. Below is a detailed analysis of each section.

1. Dynamic logic:

The dynamic logic including (M_1, M_2, M_3) and (M_4, M_5, M_6) are responsible for comparing the two input signals (IN and VCDL) based on their phase difference. These transistors operate dynamically, where the drain node of M_1 is precharged to VDD and then conditionally discharged during evaluation. The architecture defines the minimum detectable phase difference, which in turn determines the overall precision of the PFD.

2. Multiplexer:

The multiplexer directs the appropriate signal to the output based on the phase comparison. (M_7, M_8) and (M_9, M_{10}) acts as multiplexers. It processes the Up and Down signals, ensuring that only one is active at any given time. The CMOS-based structure enables high-speed switching with minimal propagation delay. The multiplexer ensures that the circuit operates correctly within a DLL, preventing unwanted glitches [23-27].

3. Voltage Level Buffers:

The buffer section enhances the voltage levels of the output signals. The transistors (M_{11}, M_{12}) and (M_{15}, M_{16}) act as buffers. These transistors adjust the output voltage levels to ensure compatibility with subsequent circuit stages, such as the charge pump in a DLL. The buffers supply sufficient current to drive the subsequent stages. The design ensures proper signal levels, preventing unwanted voltage drops and maintaining output stability.

Here, the operation of the PFD is analyzed as follows:

When IN=0, the transistor M_1 is turned on, the capacitor connected to its drain (C_p) begins to charge through the VDD supply path. The charging equation for it is as follows:

$$V_{cp}(t) = V_{DD}(1 - e^{\frac{-t}{\tau}}) \quad (1)$$

Where $\tau = R_p \times C_p$ and the resistance value in the equivalent charging path is denoted as R_p.

When IN and VCDL are at logic low, transistors M_8 and M_{10} turn on, and due to their source connections to the inputs, a logic low is generated.

When IN=1 at time t_s, the multiplexer is activated, the drain capacitor is connected to the output and transfers its charge to the output load. This process can be modeled as an RC discharge circuit:

$$V_{out}(t) = V_{cp}(t_s)e^{\frac{-t}{\tau_{out}}} \quad (2)$$

where $\tau_{out} = R_{on} \times C_p$ and the resistance in the on-state of the switching transistors in the multiplexer is denoted as R_{on}. It is worth noting that CMOS buffers improve the output voltage.

When the VCDL signal is high (i.e., '1'), the capacitor is discharged through the transistor M_3. As a result of this discharge process, the UP output is driven to zero. This behavior occurs when the transistor conducts, causing the capacitor to release its stored charge, which pulls the node to a low voltage level and disables the UP signal.

Similarly, the DOWN signal is generated, while transistors (M_{13}, M_{14}) and (M_{17}, M_{18}) operate as buffers.

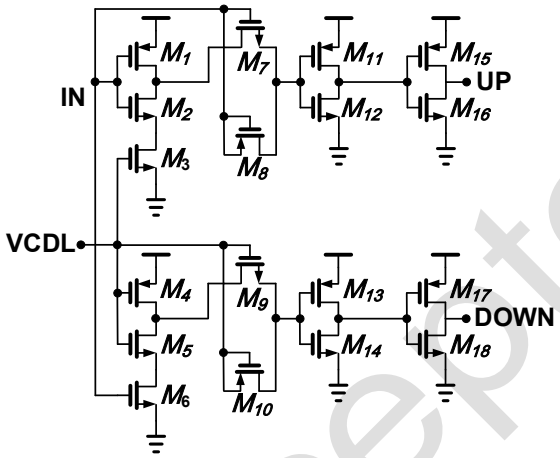


Figure 2. The proposed PFD.

2.2 Proposed CP Circuit

This circuit shown in the Figure 3 represents a CP used in the DLL systems to control the charging and discharging of the loop filter capacitor. The design incorporates gain-boosting using cascode amplifiers to enhance current matching and improve the DC-gain.

Advantages of this design are mentioned as follows:

1- Low power consumption (suitable for low-power DLLs)

2- Good current matching between charge and discharge paths

3- High DC-gain due to cascode amplifier implementation

4- Operation in high-frequency ranges (GHz-Range)

In the design of the proposed CP, the transistors labeled as (M_1, M_2) are configured as current sources, providing the necessary current flow for the circuit. The transistors (M_3, M_4) function as control switches, enabling the regulation of current distribution within the circuit. The gain-boosting architecture is achieved through the inclusion of M_5 in combination with the cascode amplifier formed by (M_7, M_8, M_9, M_{10}). Additionally, a similar gain-boosting structure is replicated by M_6 and the transistors $(M_{13}, M_{14}, M_{15}, M_{16})$, further enhancing the circuit's performance by stabilizing the gain across varying operating conditions.

A group of transistors, namely (M_{10}, M_{11}, M_{12}), along with another set of transistors (M_{16}, M_{17}, M_{18}), are configured as current sources. These current sources are capable of providing non-linear current gain, as discussed in [28-29]. Lastly, M_{19} serves as the current reference, ensuring stable and accurate current supply for the circuit. The CP output resistance is obtained from equation (3).

$$R_{out} = (g_{m5}r_{o5}g_{m3}r_{o3}r_{o1})(A_b)||(g_{m6}r_{o6}g_{m4}r_{o4}r_{o2})(A_b) \quad (3)$$

In this expression, g_m and r_o represent the transconductance of the transistor and its drain-source resistance, respectively. The transconductance g_m is a measure of how effectively the transistor can control the output current in response to changes in the input voltage, while r_o is the intrinsic resistance between the drain and source terminals, which characterizes the transistor's behavior in the saturation region. The parameter A_b denotes the gain of the cascode amplifier, which is a critical factor in determining the amplification capability of the circuit. The gain of the amplifier, A_b, is calculated using the following equation:

$$A_b = g_{m7}.R_o \quad (4)$$

R_o is the output resistance of the amplifier and it is calculated using (5).

$$R_o = (g_{m8}r_{o8}r_{o7}||g_{m9}r_{o9}r_{o10}) \quad (5)$$

Equation (5) shows that by increasing the output resistance through the cascode amplifier structure, the gain of the amplifier is significantly improved. This feature is particularly advantageous for the design of optimal CP structures, as it enables higher resistance utilization without adversely affecting the circuit's linearity or stability. This gain enhancement, while consuming less power, improves the circuit's performance and optimizes its efficiency. To confirm that the cascode configuration remains effective, all MOSFETs must operate in the saturation region under all voltage conditions. For any transistor to remain in saturation:

$$VDS \geq VGS - VTH = Vov \quad (6)$$

In the proposed CP, the bias voltages Vb1–Vb4 are carefully chosen to maintain sufficient voltage headroom across each transistor.

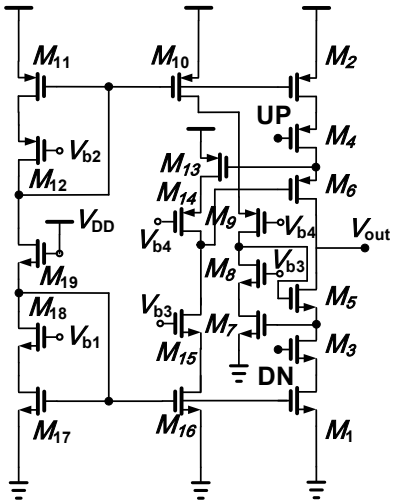


Figure 3. The proposed CP.

The current mismatch between the UP and DOWN paths is defined as:

$$\Delta I = |I_{UP} - I_{DOWN}| \quad (7)$$

Where I_{UP} is the current in the UP path when the UP transistor is on. Also, I_{DOWN} is the current in the DOWN path when the DOWN transistor is on. To achieve better current matching, the transistor current equations should satisfy:

$$I_{UP} = \beta_{UP}(V_{GS} - V_{th})^2 \quad (8)$$

$$I_{DOWN} = \beta_{DOWN}(V_{GS} - V_{th})^2 \quad (9)$$

β is the process transconductance parameter, also known as the current factor. It depends on the characteristics of the MOSFET, such as its carrier mobility and capacitance. V_{GS} is the gate-source voltage and V_{th} is the threshold voltage. The equation is a simplified model for the drain current in a MOSFET when it is operating in saturation, assuming the MOSFET is in an ideal state without considering second-order effects such as channel length modulation. For desired current matching, the following conditions should satisfy:

$$\beta_{UP} = \beta_{DOWN}, and\ V_{th,UP} = V_{th,DOWN} \quad (10)$$

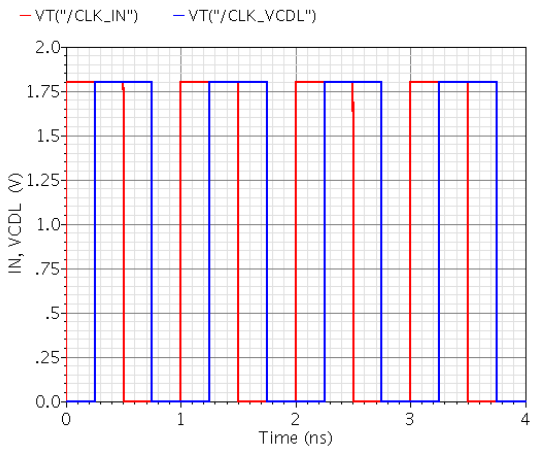
It should be noted that by increasing output resistance by gain-boosting technique, the current mismatch is reduced. This is because increasing the output resistance helps to stabilize the current and minimize the effect of small variations in transistor parameters.

3 Simulation Results

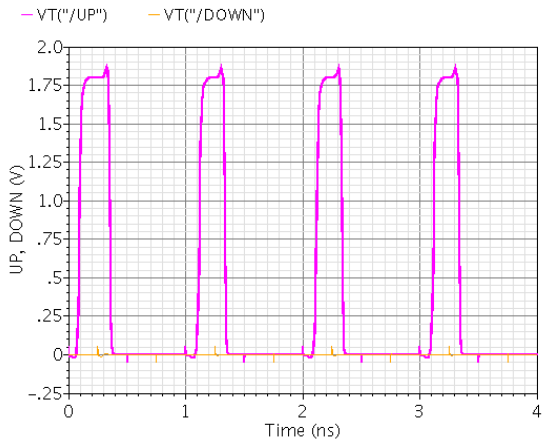
The performance of the proposed structures is validated through simulation in a 0.18 µm CMOS process with a supply voltage of 1.8 V. The simulations are carried out at both the schematic and post-layout using Cadence software. In this section, the simulation results for the dynamic PFD and CP are provided and analyzed in detail. Figure 4 illustrates the scenario where the input signal (IN) leads the VCDL. As shown in the figure, it is evident that the UP signal is set to '1', indicating the active state of the corresponding phase detector output. Additionally, the figure clearly shows that the DOWN signal remains at zero, confirming the inactivity of that output. Notably, the static power consumption of the PFD presented in this study is exceptionally low, approximately 0.4 µW, highlighting its energy-efficient design.

Figure 5 illustrates the scenario where the VCDL leads in comparison to the other input signal. In this condition, the DOWN output is observed to go high, while the UP output remains at zero, as clearly shown in the figure. These results align with the expected behavior of the PFD as detailed in Table 1. In the case where both inputs are in sync, as depicted in Figure 6, the amplitude of both the UP and DOWN outputs is close to zero, indicating a balanced condition.

The supply current waveform of the proposed design is shown in Figure 7, corresponding to the switching activity of the input signal. From this waveform, the dynamic power consumption is calculated to be approximately 7.9 µW. Figure 8 illustrates the UP and DOWN signals of the PFD operating at 3 GHz, where UP = 1 and DOWN = 0, demonstrating proper complementary switching without any overlap. These results confirm that the PFD maintains stable operation and correct logic behavior at 3 GHz, even under realistic layout parasitic conditions. The layout of the proposed PFD circuit has been designed using Cadence Virtuoso, with a layout area of 14µm×20µm, as shown in Figure 9.



(a)



(b)

Figure 4. PFD Performance: (a) The input signal (IN) is leading in comparison to the other input signal, (b) The corresponding UP and DOWN signals are shown (UP='1' and DOWN='0').

The Figure 10 illustrates the phase noise response of the PFD. This characteristic serves as a key metric for evaluating the stability and spectral purity of the output signal generated by the PFD.

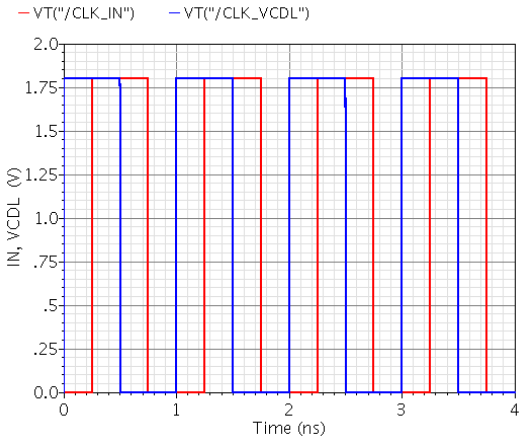
As can be observed, at low offset frequencies the phase noise level is approximately -110 dBc/Hz. With increasing frequency offset, the phase noise decreases steadily, indicating a consistent and well-controlled noise performance across a wide frequency range. This downward trend highlights the ability of the circuit to maintain high signal integrity over varying operating conditions. At offset frequency of 1 MHz, the phase noise is -162.3 dBc/Hz. Achieving such a low noise level demonstrates the superior performance of the PFD and underlines its suitability for high-precision applications. This is of particular importance in the DLL and communication systems, where signal stability and spectral purity are critical requirements. Overall, the simulation results confirm that the investigated PFD provides an excellent phase noise performance, particularly at high offset frequencies. This performance ensures the applicability of the circuit in advanced frequency synthesis and communication systems that demand high signal quality and low noise operation.

The performance of the proposed PFD is compared with that of existing competitors, and the results are summarized in Table 2. The proposed structure demonstrates lower power consumption compared to the current alternatives, primarily due to the incorporation of CMOS inverters, which enhance its energy efficiency. Additionally, a significant advantage of the proposed design over the existing techniques is its ability to operate across a broader frequency range, offering greater flexibility and performance in a variety of applications.

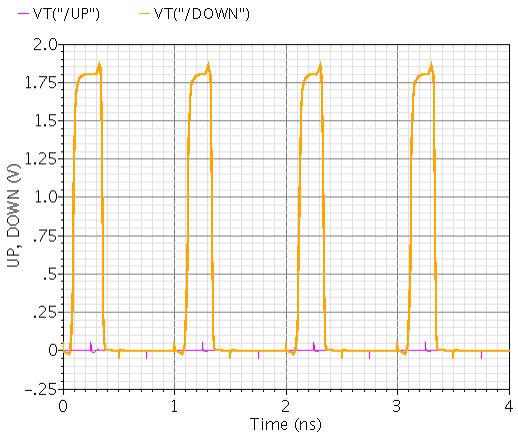
The output currents, I_{UP} and I_{DOWN}, associated with the proposed CP circuit under different process and temperature corners—TT (27°C), FF (-40°C), and SS (90°C)—are presented in Figure 11. The figure illustrates that the mismatch between the output currents is less than 3%, which highlights the high performance and reliability of the circuit across varying conditions.

Monte Carlo (MC) simulations of the proposed CP are performed considering both process variations and mismatch. Figure 12 shows the MC histograms of I_{UP} based on 100 simulation runs. From Figure 12, the mean and standard deviation of I_{UP} are 101.2 µA and 2.8 µA, respectively. For I_{DOWN} (Figure 13) the mean and standard deviation are 102.1 µA and 3.8 µA, respectively. The current mismatch between I_{UP} and I_{DOWN} is less than 3%. The layout of the CP is shown in Figure 14, with a total area of 16µm×17µm, emphasizing its compact design.

Table 3 demonstrates that the proposed CP exhibits a smaller current mismatch compared to the existing designs. In particular, the mismatch of the proposed CP is less than 3%, whereas the conventional architectures [19-20] show 3.2% and 5.4%, respectively. This noticeable improvement confirms the superior current matching and enhanced performance of the proposed design.

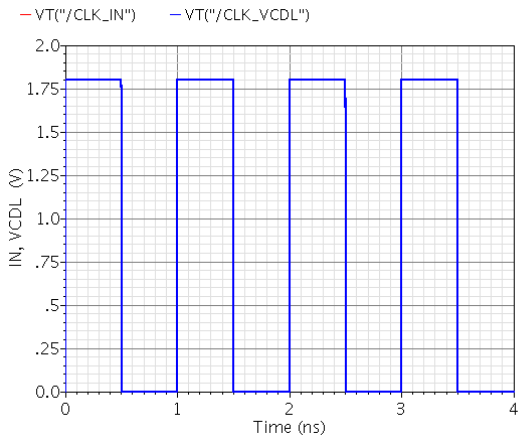


(a)

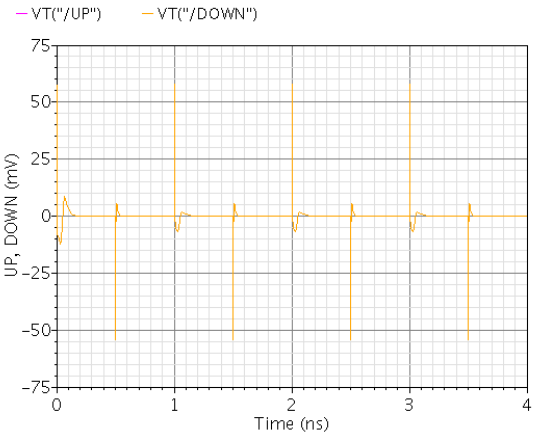


(b)

Figure 5. PFD Performance: (a) VCDL is leading in comparison to the other input signal, (b) The corresponding UP and DOWN signals are shown (UP='0' and DOWN='1').



(a)



(b)

Figure 6. PFD Performance: (a) Both input signals are matched, (b) The corresponding UP and DOWN signals are shown (UP='0' and DOWN='0').

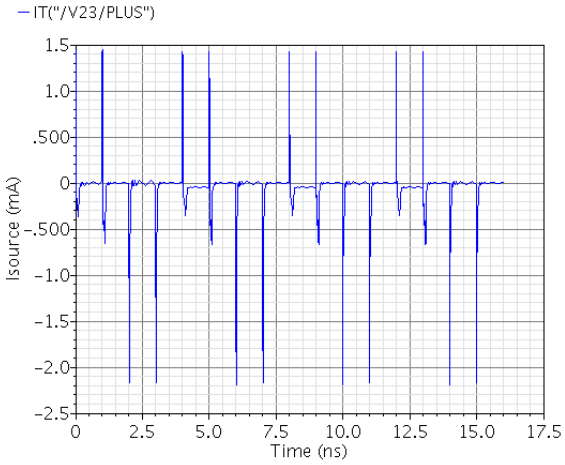


Figure 7. Supply current waveform of the proposed design.

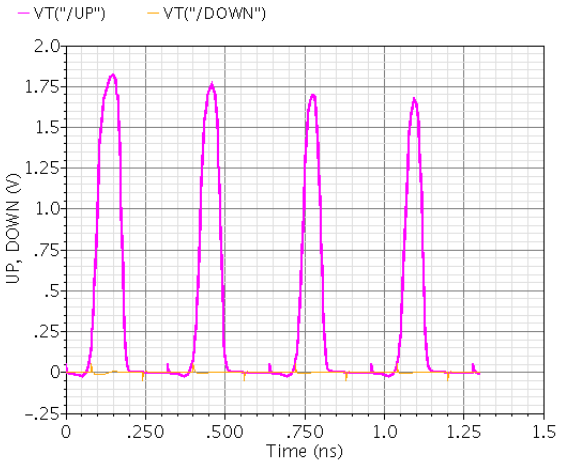


Figure 8. UP and DOWN signals of the PFD at 3 GHz, showing complementary switching without overlap.

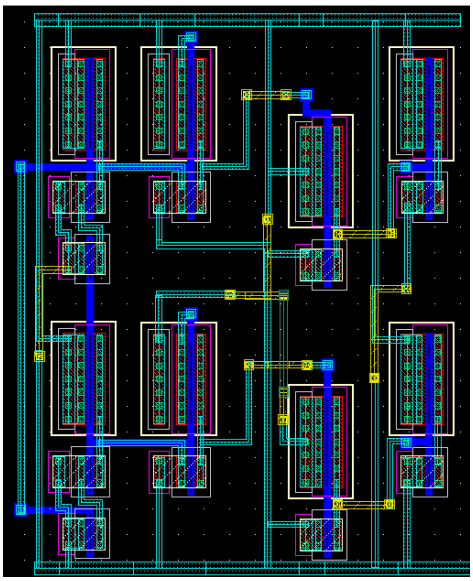


Figure 9. Layout of the PFD.

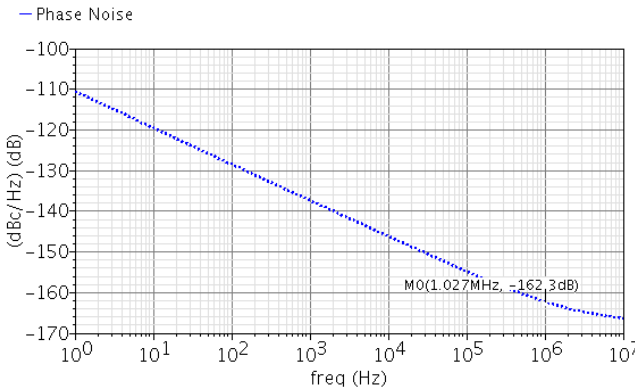
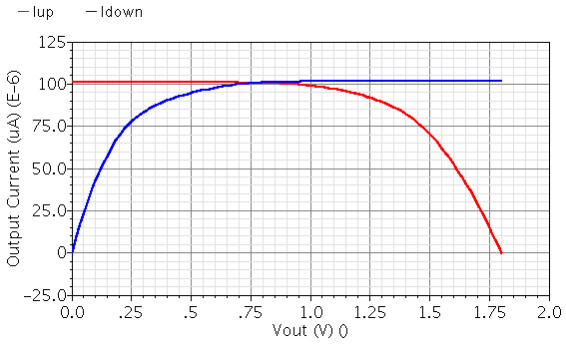


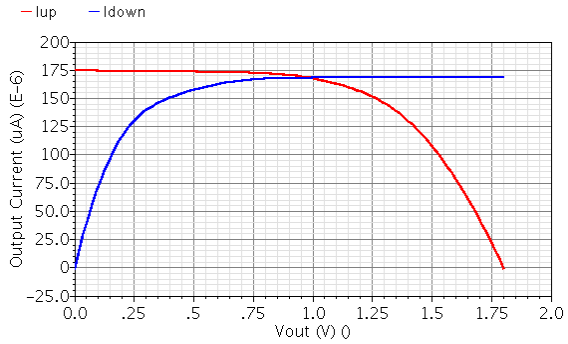
Figure 10. Phase Noise of the PFD.

Table 2. Comparison parameters of the proposed PFD and existing PFDs.

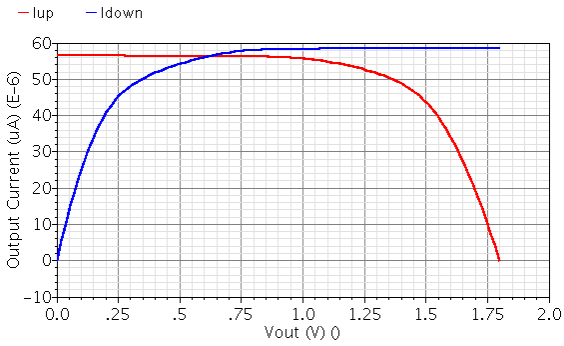
Design specifications	[27]	[26]		[21]	PFD
Technology	180 nm	180 nm		90 nm	180 nm
Power supply voltage	1.8 V	1.8 V		1 V	1.8 V
Dynamic Power Consumption (μW)	500	25		11	7.9
Static Power Consumption (μW)	--	--		--	0.4
Maximum operating frequency (GHz)	1	0.65		1	3
Area (μm²)	304	221		156	280



(a)



(b)



(c)

Figure 11. The output currents of the proposed CP circuit under different process and temperature corners. a) TT(27°C), b) FF(−40°C), c) SS(90°C).

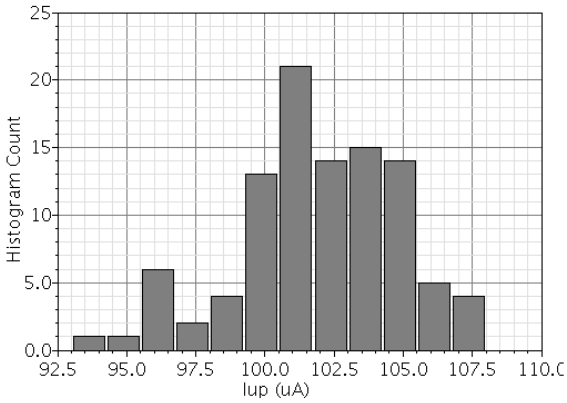


Figure 12. Histogram of Monte Carlo Simulation for I_{UP} of the Proposed CP.

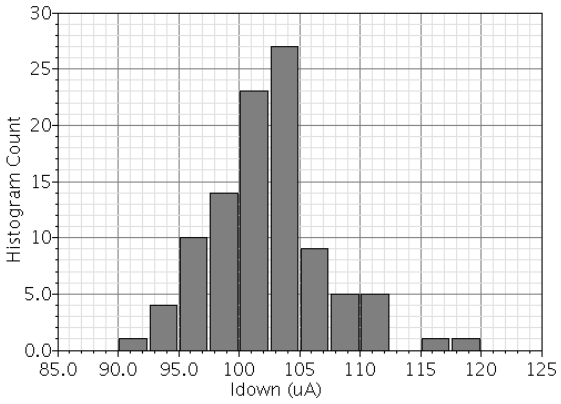


Figure 13. Histogram of Monte Carlo Simulation for I_{DOWN} of the Proposed CP.

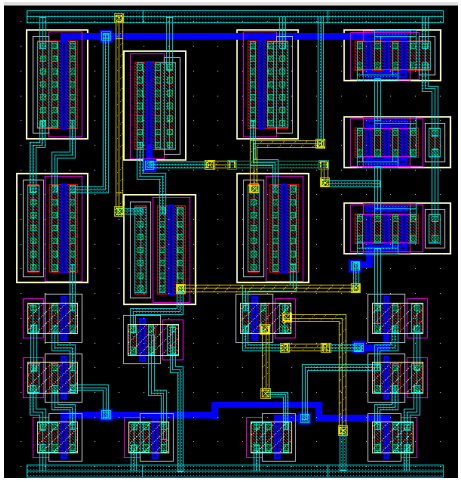


Figure 14. Layout of the CP.

Table 3. Comparison of current mismatch between the proposed and existing charge pump circuits.

	Proposed CP	[19]	[20]
Technology	180 nm	130 nm	40 nm
Supply Voltage (V)	1.8	1.2	1.2
Current Mismatch	3%	3.2%	5.4%

4 Conclusions

In this paper, a novel dynamic PFD implemented in a 0.18 µm CMOS process is presented. The design operates with a supply voltage of 1.8 V, utilizing CMOS inverters as the core building blocks. Simulation results demonstrate that the proposed PFD can operate at significantly higher frequencies—approximately 3 GHz—compared to existing competitors, which highlights its superior performance in high-speed applications. Additionally, the power consumption of the proposed PFD is exceptionally low, around 0.4 µW, which makes it highly energy-efficient. While the area of the proposed PFD is slightly larger than that of existing designs, the increase is minimal and is a trade-off for the improved performance. Furthermore, a new CP based on a gain-boosting technique is introduced, which exhibits excellent current matching, with a mismatch of less than 3%. This feature contributes to the overall reliability and stability of the system. The proposed circuits have been integrated into a DLL, where their high efficiency and effectiveness were confirmed. These results indicate that the combination of the proposed PFD and CP circuits provides a promising solution for applications requiring high-speed, low-power, and reliable performance. The paper offers valuable insights into optimizing PFD and CP designs for next-generation frequency synthesis and timing circuits.

Conflicts of Interest:

The authors declare no conflict of interest.

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